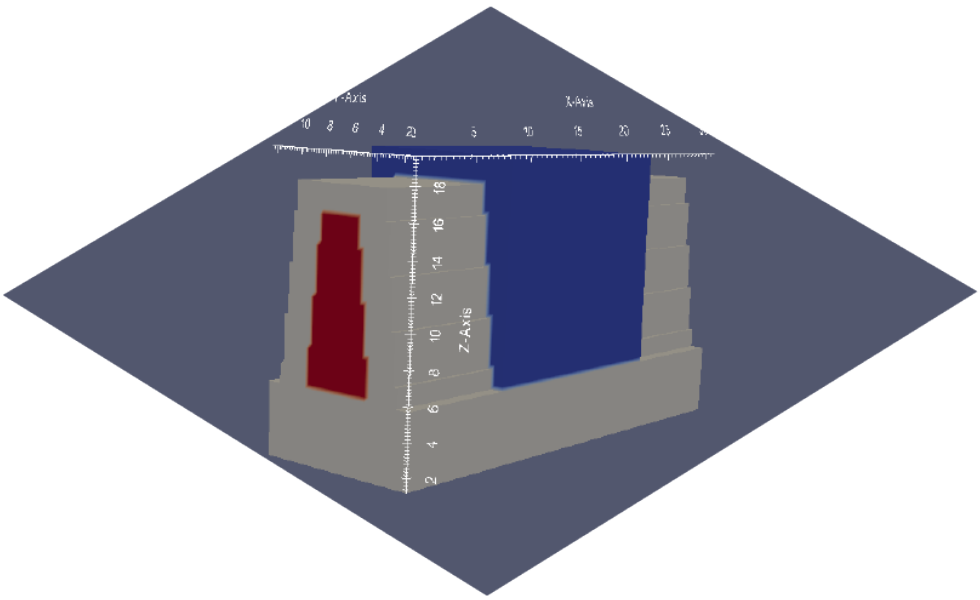
Silicon FinFET

EOLAS Designs

Abstract

In this document we demonstrate some of $\mathcal{M}^*$'s capabilities by simulating the properties of a silicon fin field-effect transistor (FinFET).

FinFETs are employed as digital switches in modern integrated circuits where they have increasingly replaced planar MOSFET designs over the past decade due to their increased performance springing from the improved electrostatic control of the channel allowed by such designs. In this tutorial we simulate the electrical properties of a silicon FinFET with sub 10 nm geometrical features, and a gate length of 15 nm. With present technology nodes already comprised of similar device geometries at slightly larger dimensions, devices similar to the FinFET presented here may be a reality in the next few years.



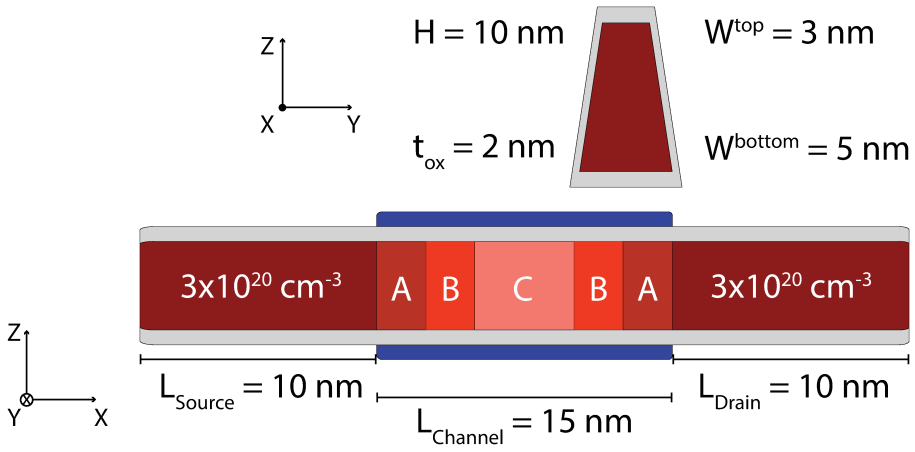


Figure 1: Schematic indicating the geometrical dimensions and doping profile of the simulated device.

$\mathcal{M}^*$ performs device simulations based on fully quantum-mechanical electronic structure models in tandem with a non-equilibrium Green's function (NEGF) approach for charge transport. $\mathcal{M}^*$'s implementation enables FAST simulation of device properties for quick turnaround design times; results presented in this document have been obtained in around 40 minutes using a single processor core on a modern laptop.

A schematic describing the geometry and doping profile of the device at hand is shown in fig. 1. The device is comprised of a cylindrical [110] silicon nanostructure with a trapezoidal cross-section with a top width of 3 nm, bottom width of 5 nm, and height of 10 nm. The gate electrode is electrically insulated from the channel by a 2 nm thick layer of high-κ oxide; a 15 nm long channel region is defined by a gate electrode surrounding the fin in a tri-gate architecture. The wide contacts acting as the device's source and drain are not explicitly modelled as they are assumed to be far away from the device channel and have ideal contacts (i.e. ohmic contacts) to narrow lead extensions located on either side of the channel, as per the usual NEGF framework.

In order to account for electrostatic screening and its effects on the device's electrical properties, we explicitly model portions of the lead extensions closer to the gate electrode. The required length of lead extensions to be explicitly modeled depends on the materials comprising the device, its geometry and doping profile; for this design all properties are converged for lead extension lengths of 8 nm. Regions coloured with varying shades of red in fig. 1 highlight variations in the doping profile: the leads extensions are doped n-type to a free electron concentration of 3×10^{20} N/cm^3 while the region under the gate emulates a doping concentration decaying into the centre of the channel: regions labelled (A) in the figure are doped to a carrier concentration of 5×10^{19} N/cm^3, regions labelled (B) to 5×10^{18} N/cm^3, and region (C) to 10^{16} N/cm^3.

Input files required for a corresponding $\mathcal{M}^*$ simulation can be prepared with the $\mathcal{M}^*$ Graphical User Interface (GUI). Figures 2 to 4 show different sections of $\mathcal{M}^*$'s GUI along with input values describing the Si FinFET device:

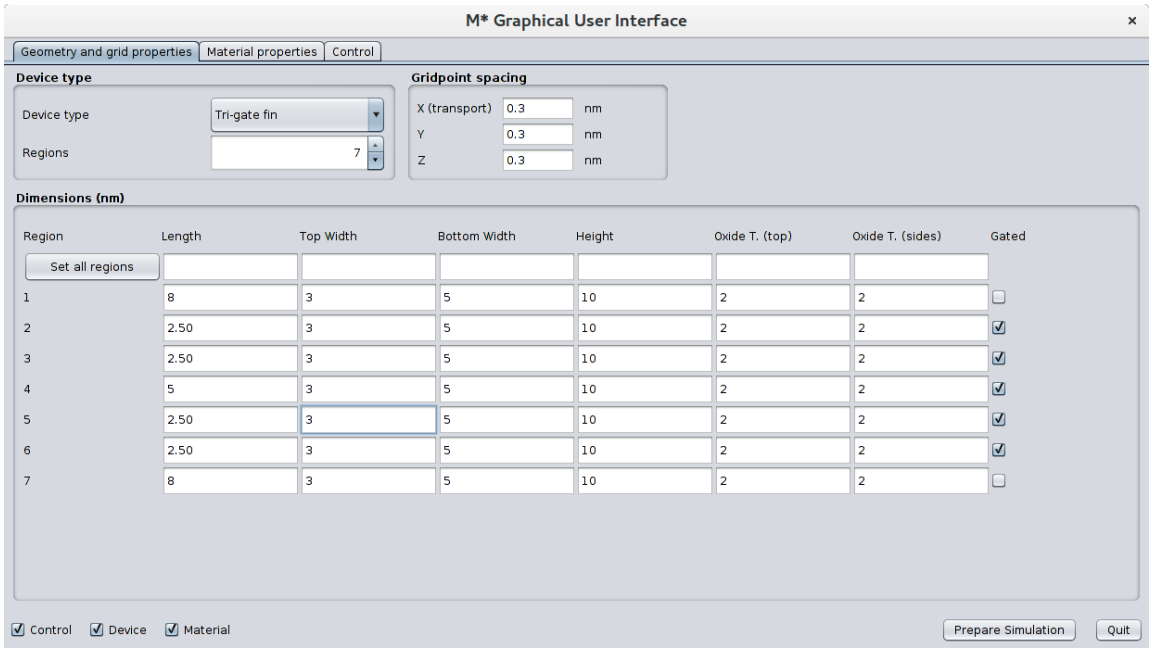


Figure 2: $\mathcal{M}^*$ Graphical User Interface: `Geometry and grid properties` tab.

- The `Geometry and grid properties` tab defines the device as a tri-gate FinFET with seven distinct regions, and sets appropriate grid spacings
- The `Material properties` tab describes the properties of the conduction-band valleys and permittivity of each region
- The `Control` tab allows defining the type of voltage sweep and its limits, type of scattering to be considered in the simulation, convergence parameters, and files to be output

We neglect all sources of electron scattering and simulate the device in the ballistic regime, a reasonable approximation given its short length. This type of simulation quickly provides information on the device's properties as defined by its geometry and intrinsic material properties, thus allowing exploration of performance limits when sources of scattering detrimental to device operation such as electron-phonon interactions are not accounted for.

Figure 5 shows the device's transfer characteristics in a semilog and linear plots for a drain-source bias of $V_{DS} = 0.4$ Volts. A least-squares fit results in a predicted subthreshold swing (SS) of around 70 mV/dec, indicating switching characteristics between those of planar devices and nanowire devices.

In fig. 5 we have highlighted in red circles three bias points corresponding to OFF, ON, and SAT (saturation) states which we take as representative of each device operation regime for exploring evolution of other quantities shown below.

Figure 6 shows the lowest subband in energy across the device when in its OFF state (green), ON state (yellow), and in saturation regime (red). It can be seen how the barrier encountered for electrons coming from the source (left hand side in the figure) is reduced for increasing values of gate bias, thus allowing larger currents to flow through the channel. While the barrier induced in the channel region in its

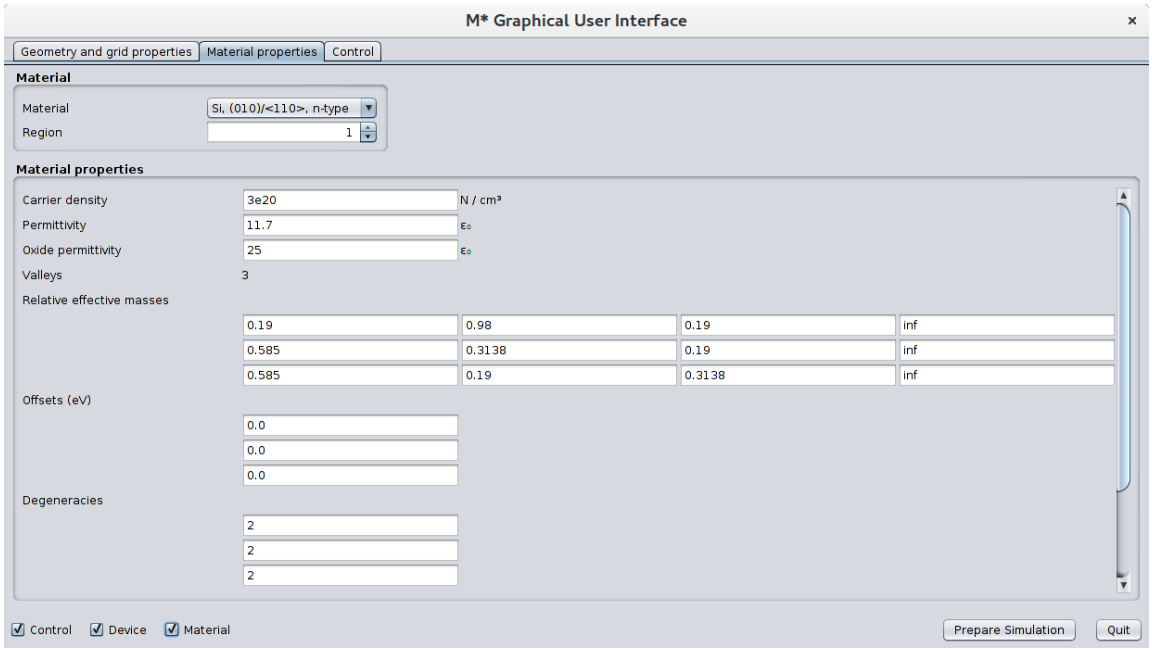


Figure 3: $\mathcal{M}^*$ Graphical User Interface: `Material properties` tab.

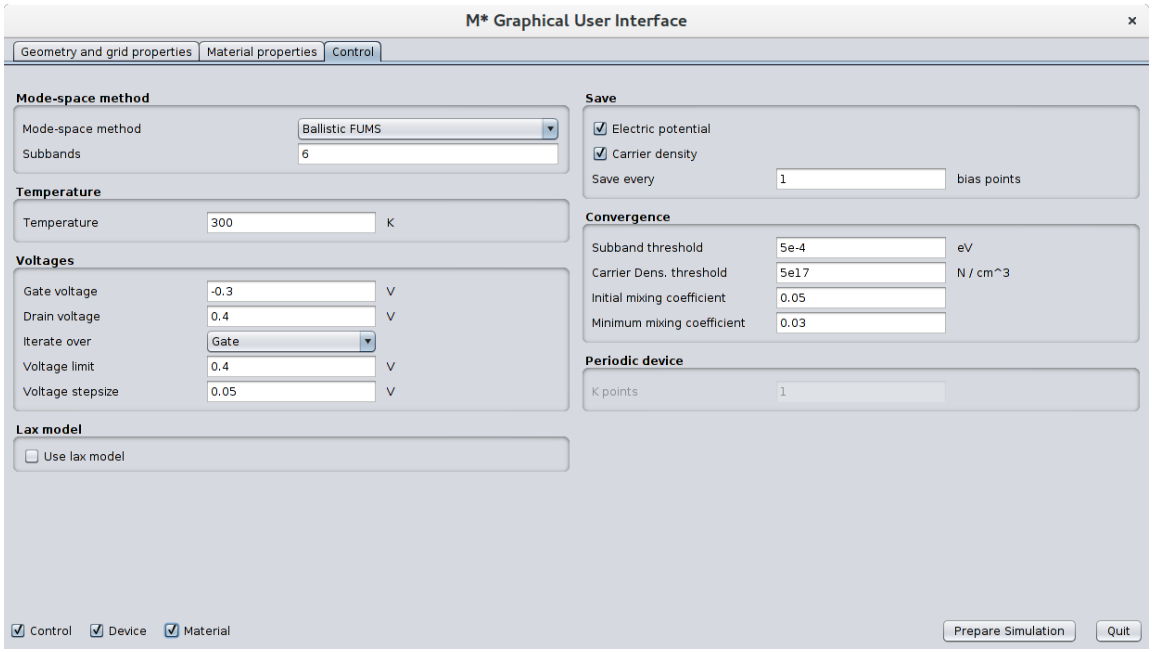


Figure 4: $\mathcal{M}^*$ Graphical User Interface: `Control` tab.

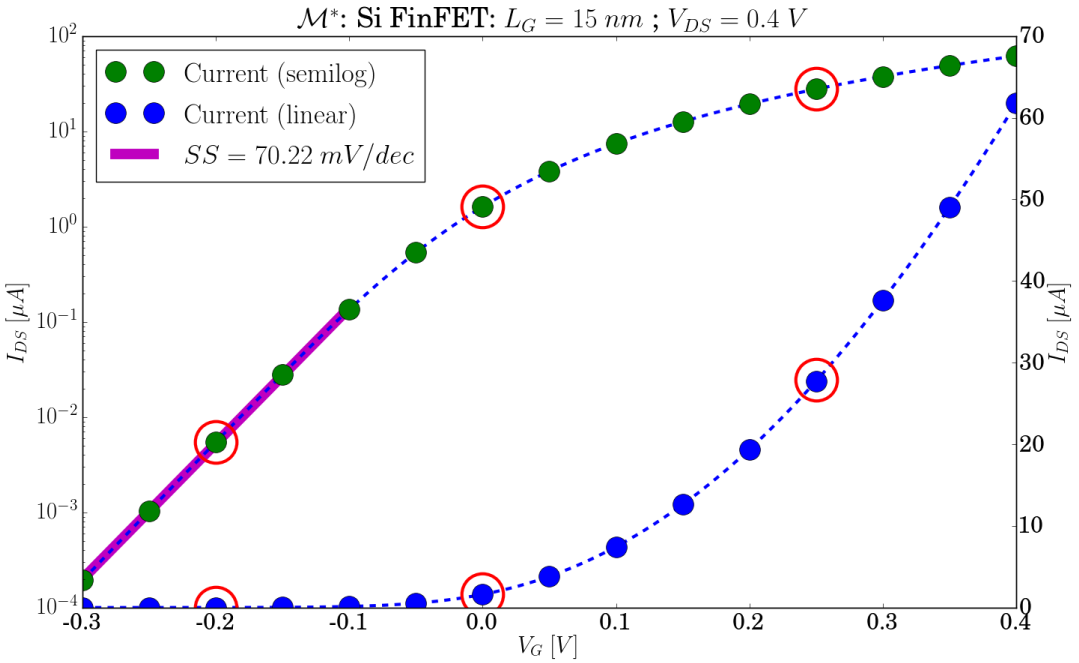


Figure 5: Si FinFET transfer characteristics.

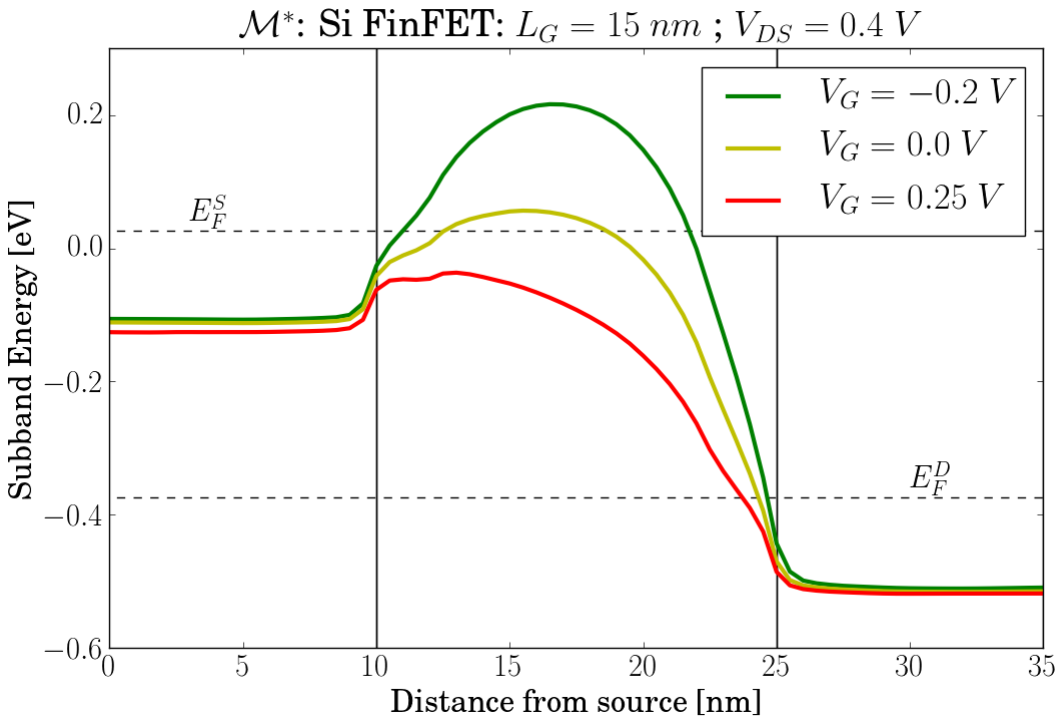


Figure 6: Evolution of lower subband in energy with gate bias.

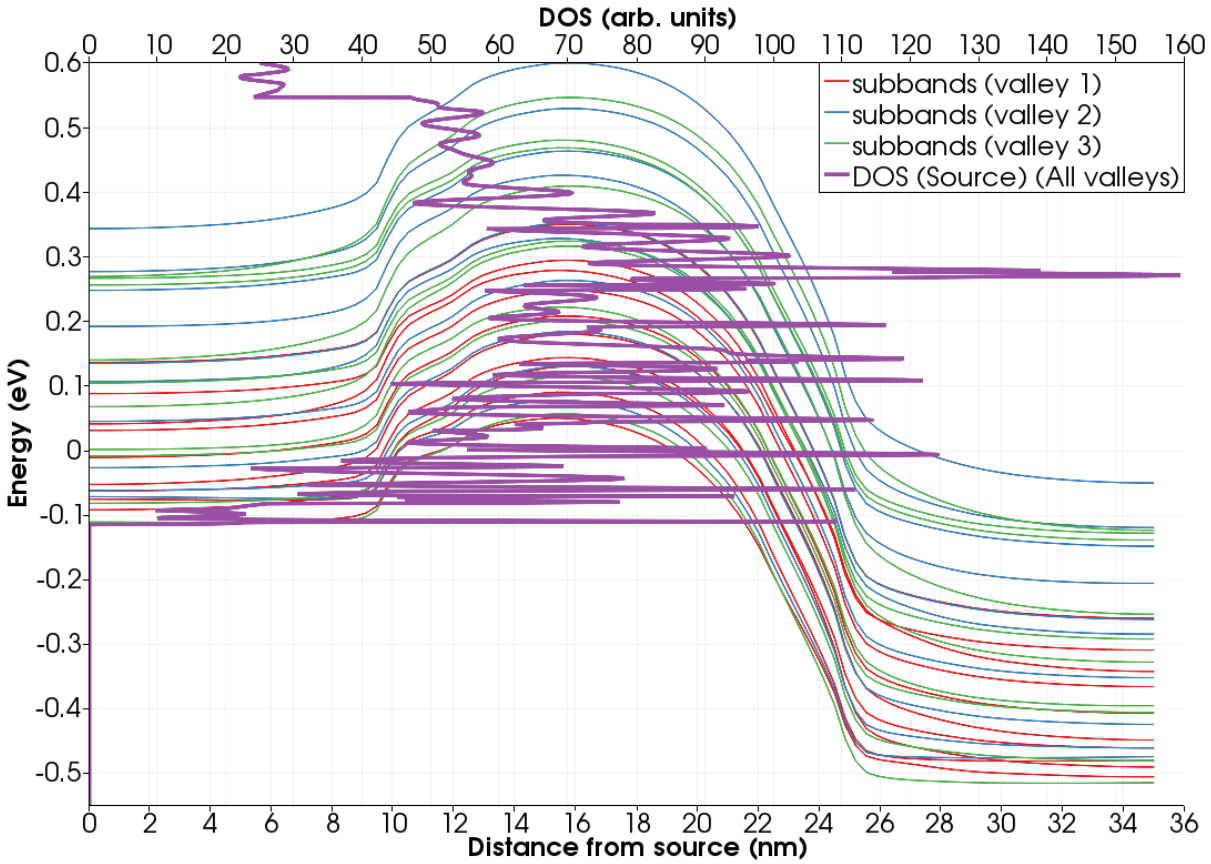


Figure 7: Subband profile and density of states at the source region for carriers in a particular conduction valley.

OFF state is over 300 meV above the source Fermi level ($\approx 15 \times \kappa_B T$ at room temperature) and severely impedes current flow, the first subband lies below the source Fermi level across the whole device when in saturation regime so electrons can easily flow through it.

$\mathcal{M}^*$ enables comprehensive analysis of simulated devices' electronic structure by allowing extraction, visualisation, and overlaying a number of results such as of density of states, subband profiles, and transmission probabilities associated to each conduction valley and device region, as depicted in figs. 7 and 8.

Additionally, you may plot the carrier density and electrostatic potential across the device as 3D grids for a better understanding of how they correlate and ultimately gain insight into device operation and design optimisation based on simulations based on quantum mechanical models.

To learn more about $\mathcal{M}^*$'s features and capabilities or to request a demo version, don't hesitate to contact us at `support@eolasdesigns.com`

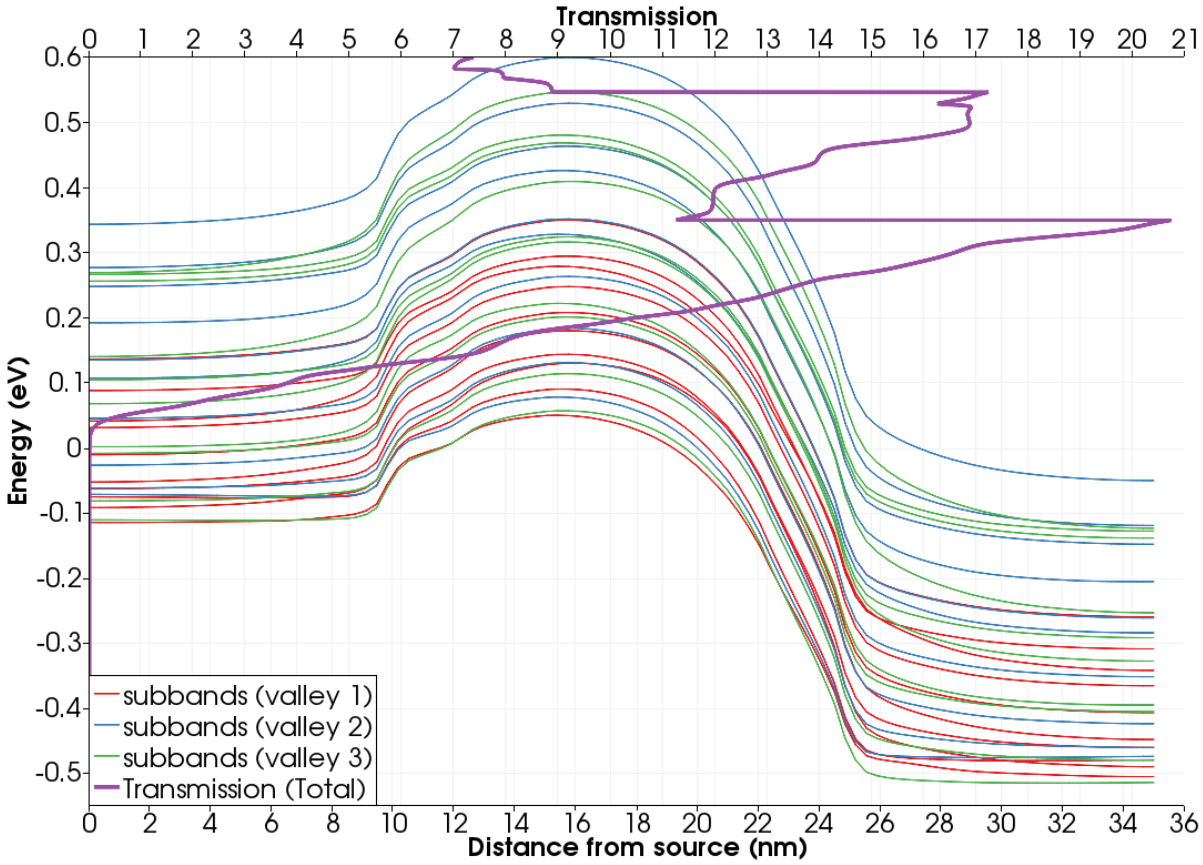


Figure 8: Subband profile and transmission probability function at the source region for carriers in a particular conduction valley.

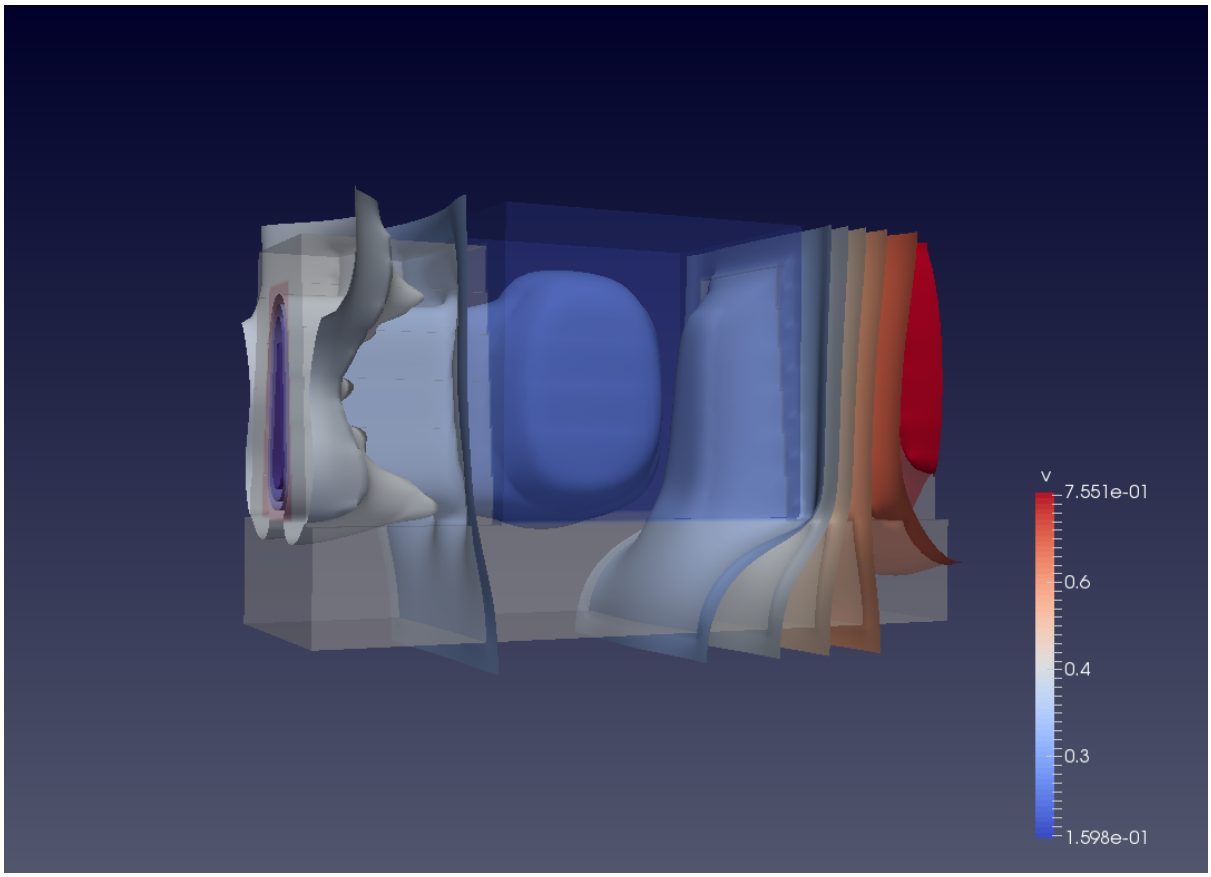


Figure 9: Electric potential isosurfaces across a Si FinFET.

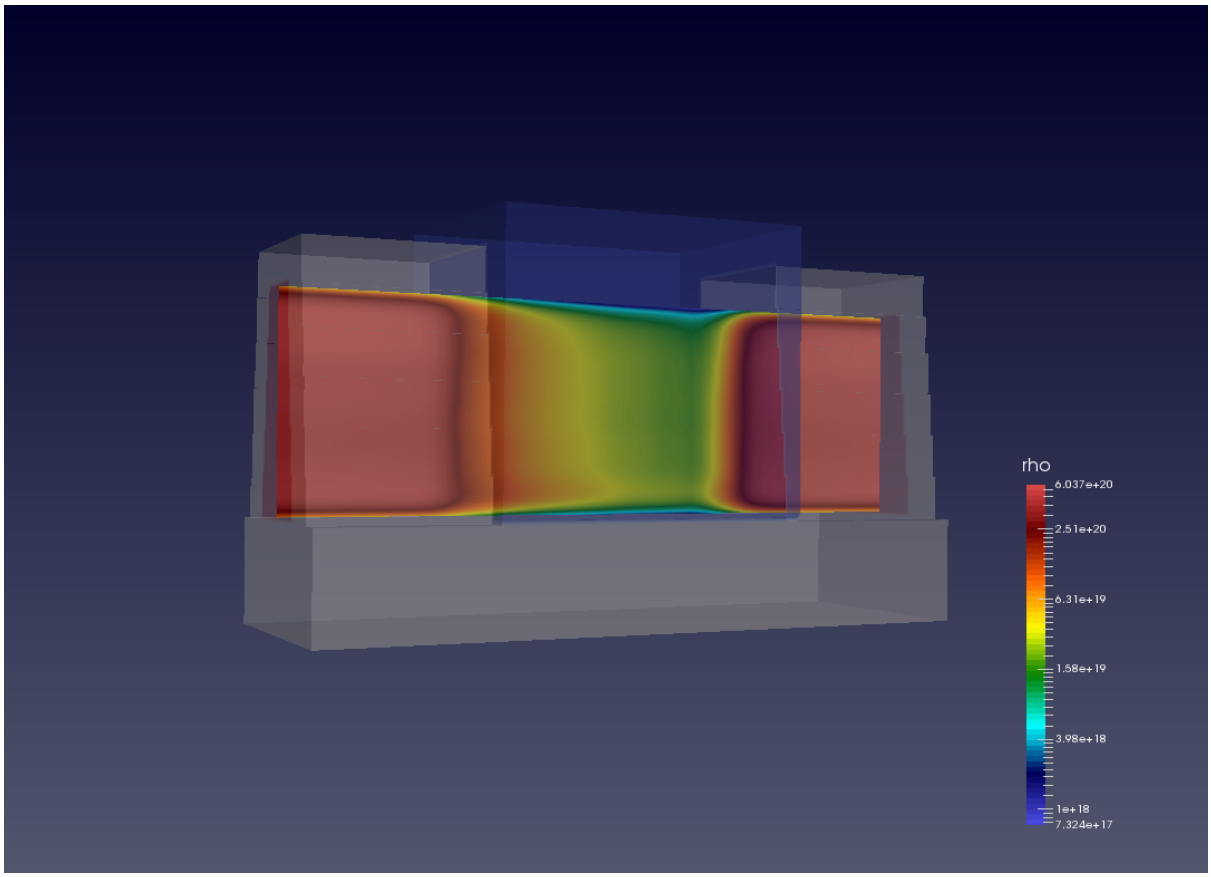


Figure 10: Carrier density through a plane crossing the centre of the FinFET.