
# The $\mathcal{M}^*$ Simulator

v3.2

## Tutorial Booklet

EOLAS Designs

## Contents





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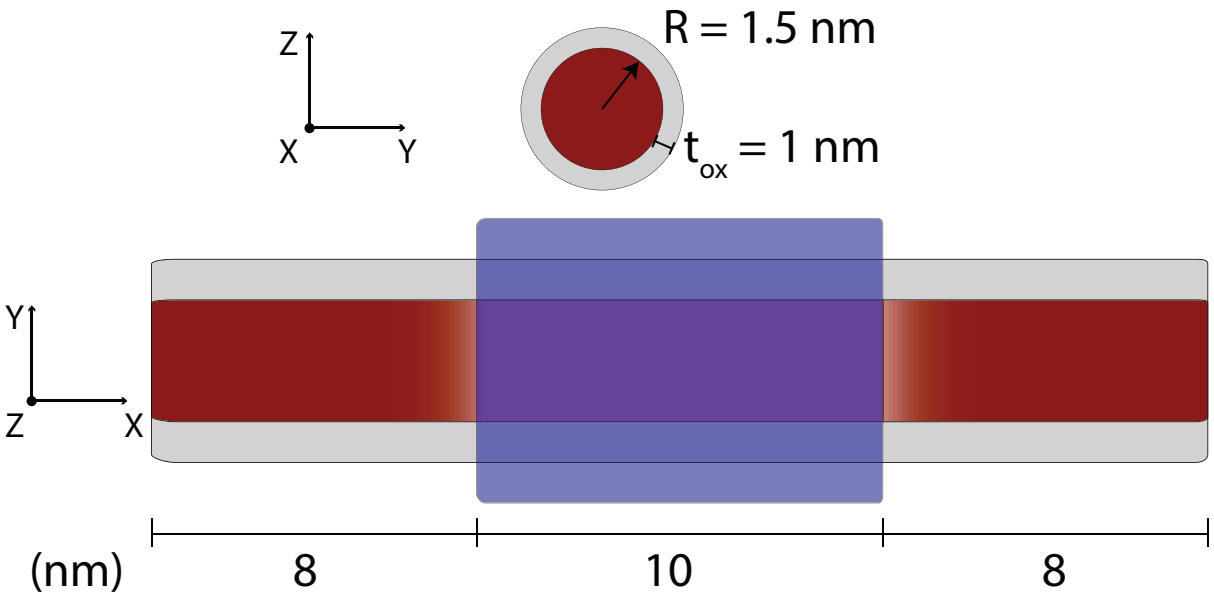


Figure 1: Si NWFET: Schematic showing device geometry. Red represents silicon, gray represents silicon dioxide, and blue the gate electrode. Regions in different shades of red represent variations in doping across different device regions.

# 1 Tutorial: Silicon nanowire FET

This section illustrates the process of preparing, running, and analysing a simulation of a silicon nanowire field-effect transistor (Si NWFET) with homogeneous geometry along its transport axis (i.e. constant cross-section) by employing the ballistic FUMS method. We shall simulate a silicon $\langle 100 \rangle$ gate-all-around device with cylindrical cross-section and a radius of 1.5 nm, a channel length of 10 nm, and 8 nm long source/drain extension regions. Figure 1 shows a schematic of the device geometry, highlighting variations in the doping profile across the silicon portion of the nanowire with different shades of red. Source and drain regions are doped n-type with a carrier concentration of $2 \times 10^{20}$ N/cm$^3$ while the channel is intrinsic with a much lower carrier density, which we shall neglect and take to be zero.

In order to begin preparing the input files for simulating this device, launch the $\mathcal{M}^*$ GUI, click `New` and choose a folder to save your results to. Navigate to the `Device` panel on the left pane and set device geometry parameters as described in fig. 1 by filling out values as shown in fig. 2. Leave `Gridpoint spacing` and `Surface roughness` fields to their default values. You may switch to the `Preview` tab to visualise the device structure and ensure it corresponds to your intended design.

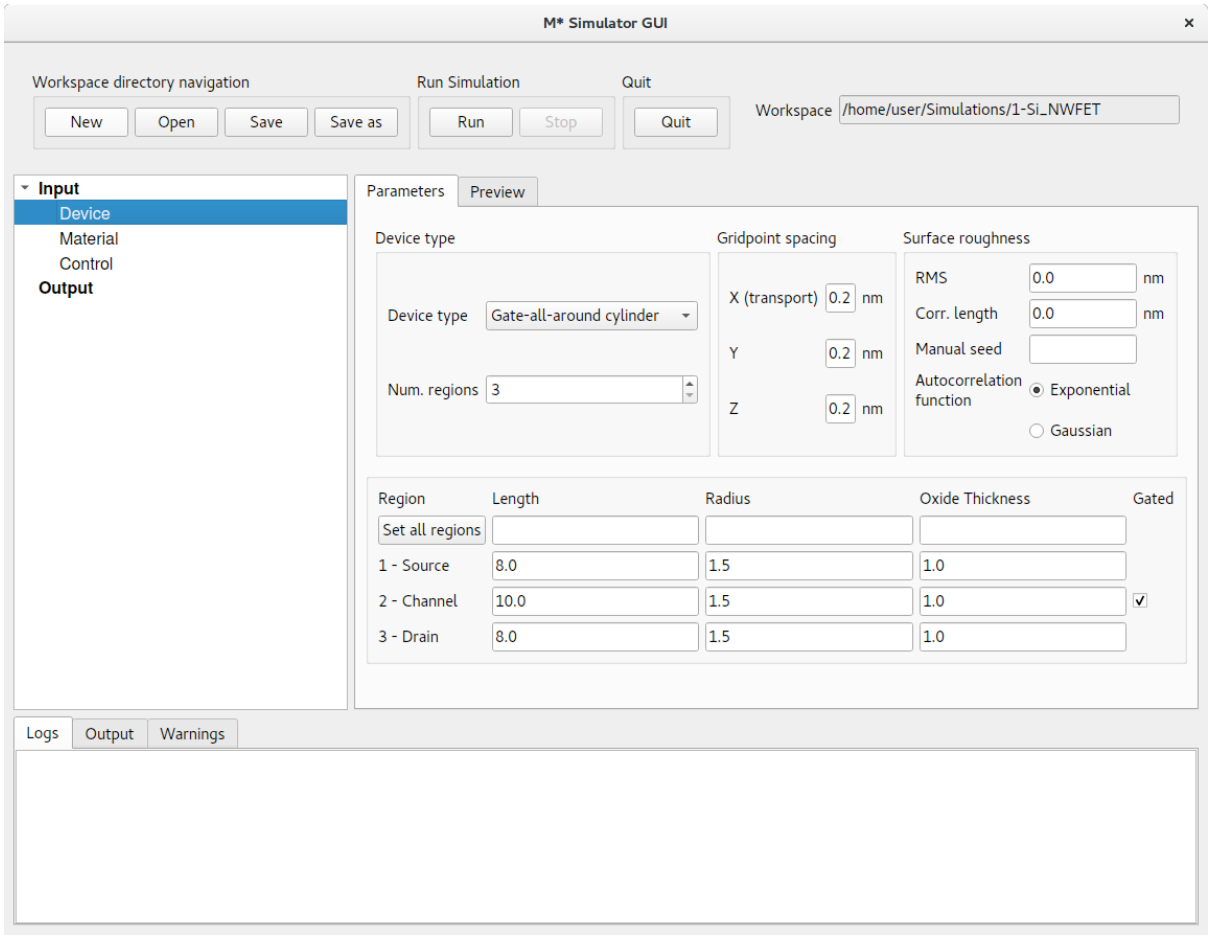


Figure 2: In the `Device` panel, specify a `Gate-all-around cylinder` with 3 regions, with dimensions shown above. Make sure region 2 (i.e. the device channel) is `Gated`.

Once you have completed filling out the `Device` panel, select `Material` in the left pane to enter the material properties for each region. Select `Si, (010)/⟨100⟩, n-type` from the dropdown menu to select the device's semiconductor material across all regions.[1] Cycle through regions 1 - 3 using the region *spinner* and ensure the oxide permittivity is set to 3.9 –the relative permittivity of silicon dioxide–, and `Carrier density` values are set as $2 \times 10^{20}$ cm$^{-3}$ for source & drain regions (regions 1 and 3) and `0.0` for the channel region (region 2). fig. 3 shows values set for the source region.

[1] Although $\mathcal{M}^*$ supports simulating devices with different materials in different regions, it requires manual editing of input files as the current version's GUI does not include support for building devices with heterogeneous materials. Selecting a material anywhere in the `Material` panel sets the main electronic structure properties for all regions.

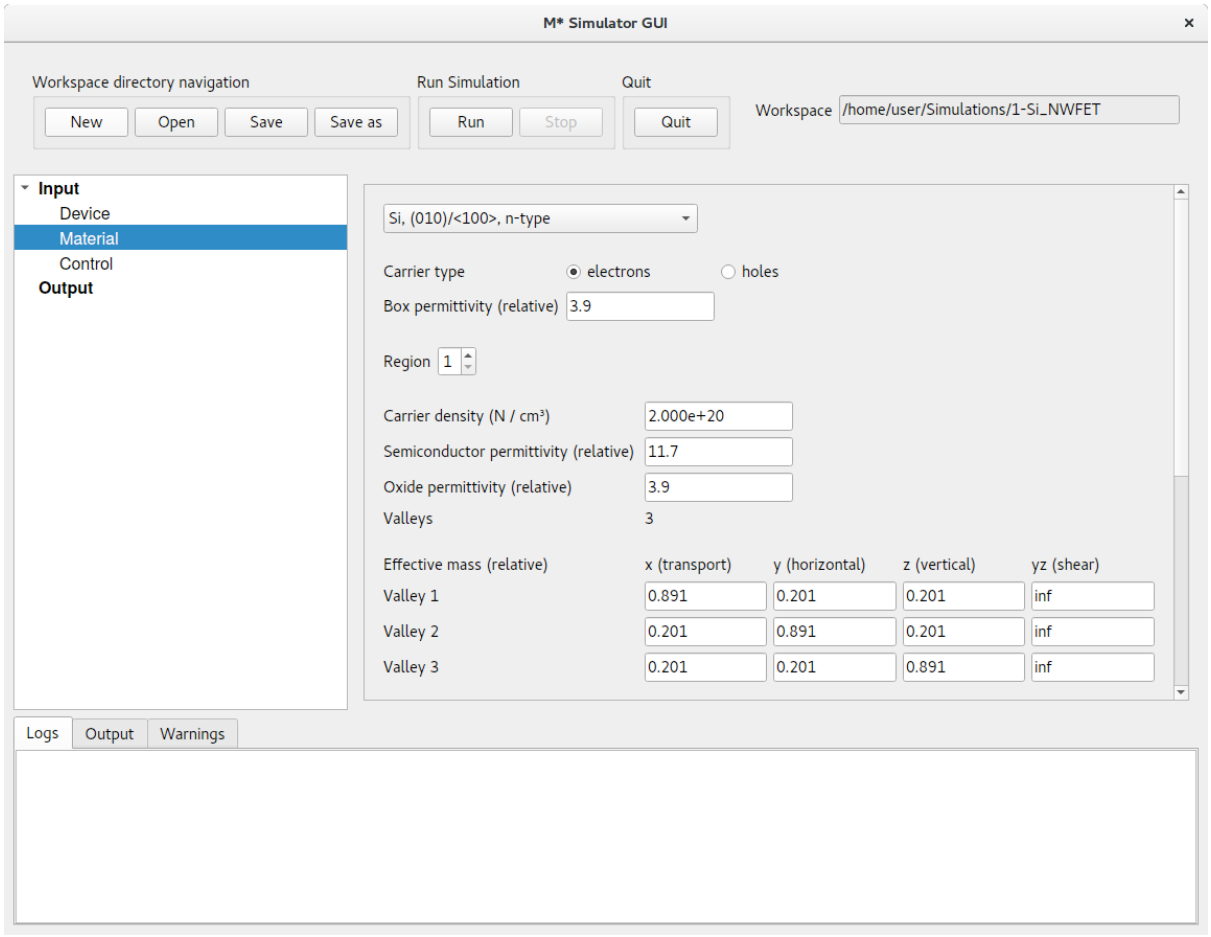


Figure 3: In the `Material` panel, cycle through regions 1 - 3 and ensure oxide permittivity is set to 3.9, and `Carrier density` values are set as $2 \times 10^{20}$ cm$^{-3}$ for source & drain regions (regions 1 and 3), and `0.0` for the channel region (region 2).

To finish setting all input parameters for our simulation, select `Control` on the left pane and fill out values as shown in fig. 4:

- **Method** select the fast uncoupled mode-space method –suitable for devices with both homogeneous and small cross-sections–, with 3 subbands per valley and `Ballistic` scattering
- **Temperature** leave a value of 300 K (26.85 °C)
- **Voltages** input a `Drain voltage` of 0.40 V and a `Gate voltage` of −0.25 V. Select `Iterate over -> Gate`, input a `Voltage limit` of 0.550 V and a `Voltage stepsize` of 0.05 V to indicate a gate bias sweep in the $[-0.25, 0.55]$ V range, in steps of 0.05 V
- **Save** enable saving of both electric potential and carrier density, and set `Save every` to 1 so data is saved for all bias points computed
- **Convergence** set the `Potential threshold` to $10^{-4}$ eV, `Carrier Dens. threshold` to 1 %, and the `Initial mixing coefficient` to 0.05. Enable `Adaptive mixing` and set the minimum and maximum coefficients to 0.01 and 0.3, respectively

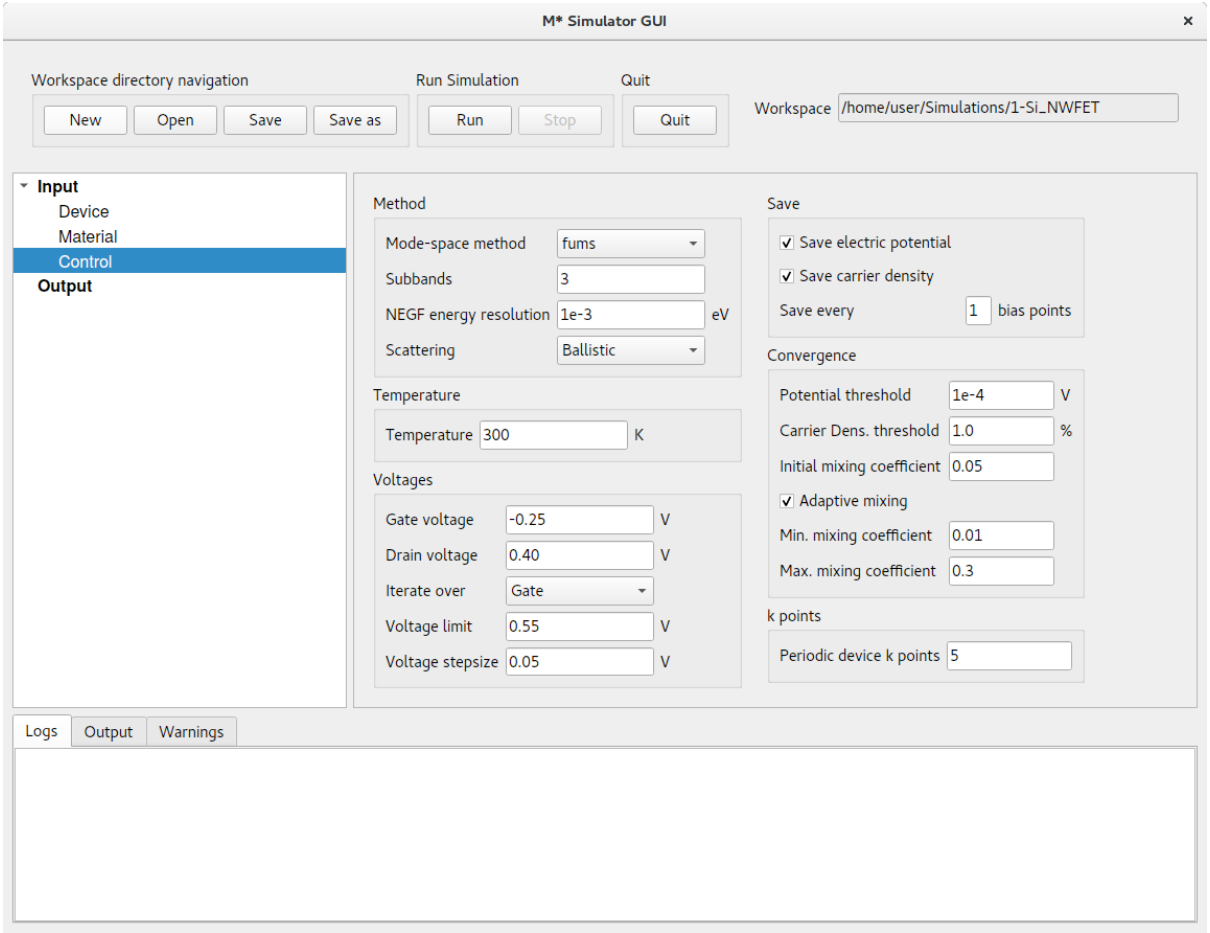


Figure 4: In the `Control` panel, fill out fields with values shown in the figure.

Once you have finished setting all input variables, you are now ready to launch your first $\mathcal{M}^*$ simulation: click `Run` at the top pane of the GUI to begin. Once your simulation has been started, a subfolder will be created inside your current workspace directory where all associated output files will be saved. You can follow simulation progress in the tabs located at the bottom pane of the GUI:

- **Logs** shows the contents of the $\mathcal{M}^*$ logfile, which is also saved to your simulation folder under the filename `mstar_log.out`. It contains a header with information about the simulated device and subsequently includes useful information on simulation progress. After each iteration, $\mathcal{M}^*$ will write a line with six columns to this file with the following quantities:
  - `Iter`: iteration index for the present bias point
  - `Vds (V)`: drain-source bias in volt
  - `Vgs (V)`: gate-source bias in volt
  - `Ids (A)`: drain-source current in ampere
  - `R[Q] (%)`: charge residue in percentage with respect to that iteration's input charge density
  - `dV (V)`: maximum difference in electric potential between the last two iterations in volt

- **Output** shows $\mathcal{M}^*$'s standard output stream `stdout`. After each iteration, the contents of this tab will get updated with the following information:
  - `Method`: mode-space method employed
  - `Drain-source bias`: drain-source bias in volt
  - `Gate-source bias`: gate-source bias in volt
  - `Drain current`: drain current in ampere
  - `Potential convergence`: maximum difference in electric potential between the last two iterations followed by the requested convergence threshold in parenthesis, both in volt
  - `Density convergence`: charge residue in percentage with respect to that iteration's input charge density, followed by the requested convergence threshold in parenthesis
  - `Linear mixing coeff`: mixing coefficient used in the present iteration
- **Warnings** shows $\mathcal{M}^*$'s standard error stream `stderr`, containing any errors or warnings that occur during the simulation

When the simulation has finished, both `Logs` and `Output` tabs will show a summary of the time taken to run the simulation, with the time spent in each $\mathcal{M}^*$ module indicated. You may then begin analysing results[2] by expanding the `Output` section on the left pane to show a list of runs performed so far in the current workspace. Every simulation launched by clicking the `Run` button will be listed under the default name `run_<N>`, with `<N>` an incremental index (e.g. `run_0`, `run_1`, etc.), and the corresponding output data will be saved to subfolders with the same name. Expand the item labelled `run_0` to list output quantities associated with the simulation just performed:

[2]Results for each bias point become available for analysis as soon as they have been converged

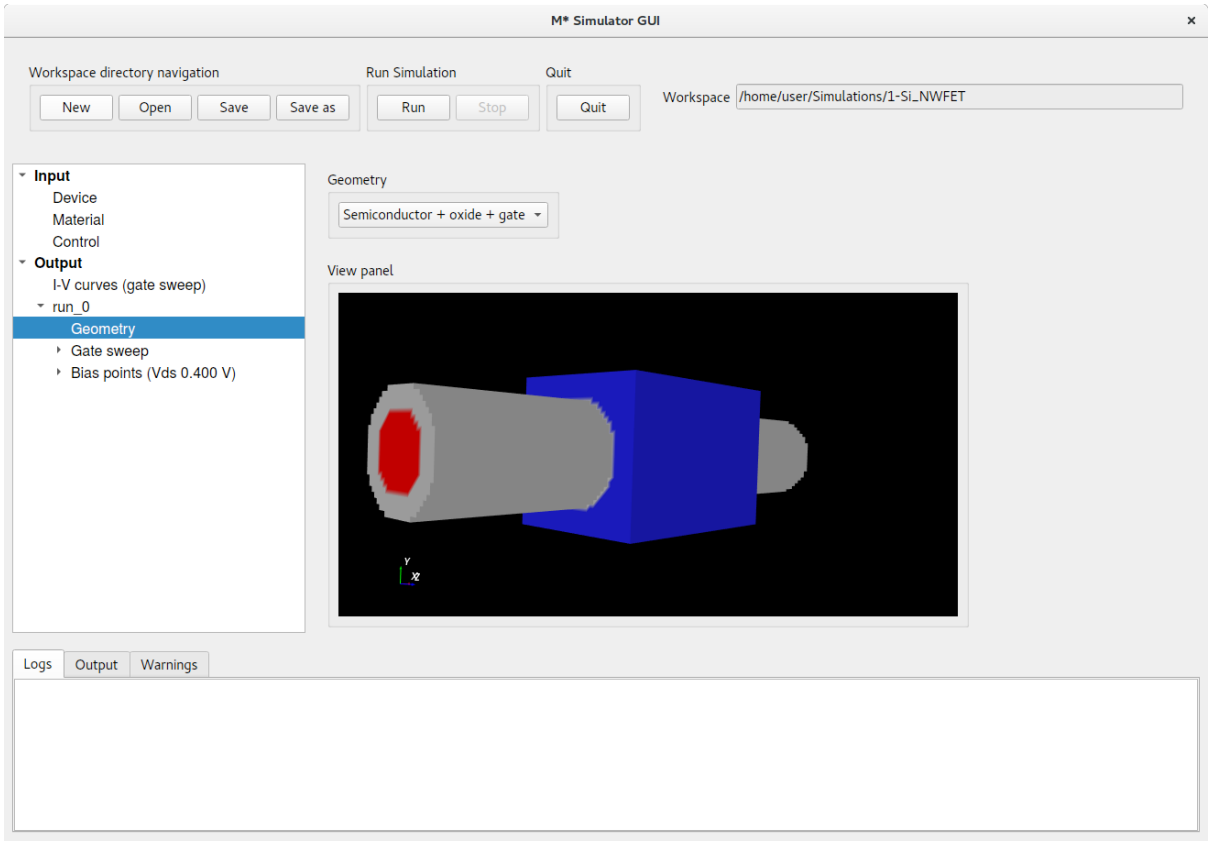


Figure 5: Once your simulation has finished running, expand the `Output` section on the left pane to list all available runs; select `run_0` to list all output corresponding to the first simulation just completed. Clicking `Geometry` displays a 3D render of the simulated device geometry.

- **Geometry** allows visualising a 3D render of the simulated device geometry, as shown in fig. 5. A drop-down menu allows choosing between visualising only the semiconductor region, the semiconductor and oxide regions, or all regions including semiconductor, oxide, and gate electrode. You may rotate the 3D model using your mouse's left click button, zoom in or out by holding your mouse's right click button, pan using your mouse's middle button (or `shift` + left click), and spin using `ctrl` + left click

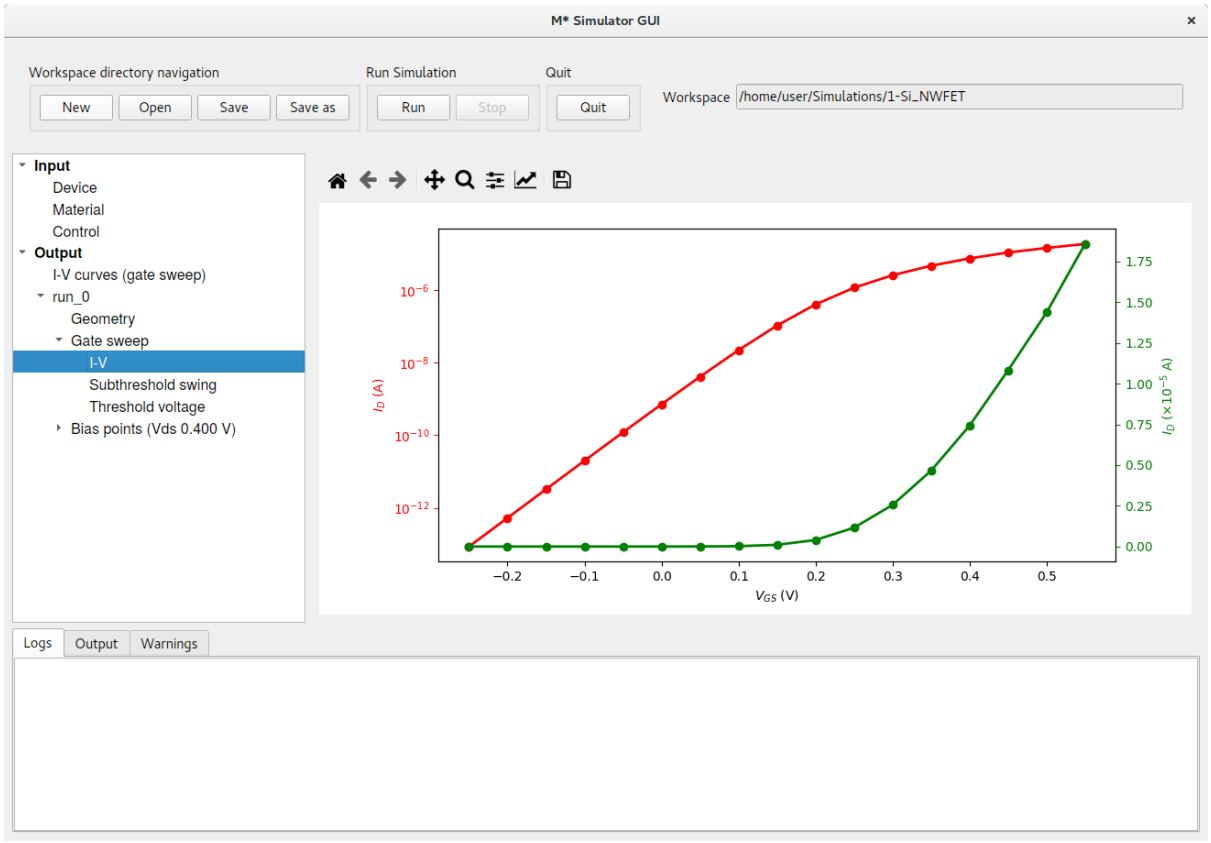


Figure 6: Device transfer characteristics are displayed as both semilogarithmic (red, left vertical axis) and linear plots (green, right vertical axis).

- **Gate sweep** expand this item to list the following output available for gate sweep runs:
  - **I-V** displays a plot of the device's transfer characteristics as both semilogarithmic and linear plots, as shown in fig. 6. The toolbar at the top of all 2D plots in $\mathcal{M}^*$ allows customising the look of the plot and save it as an image file in various formats

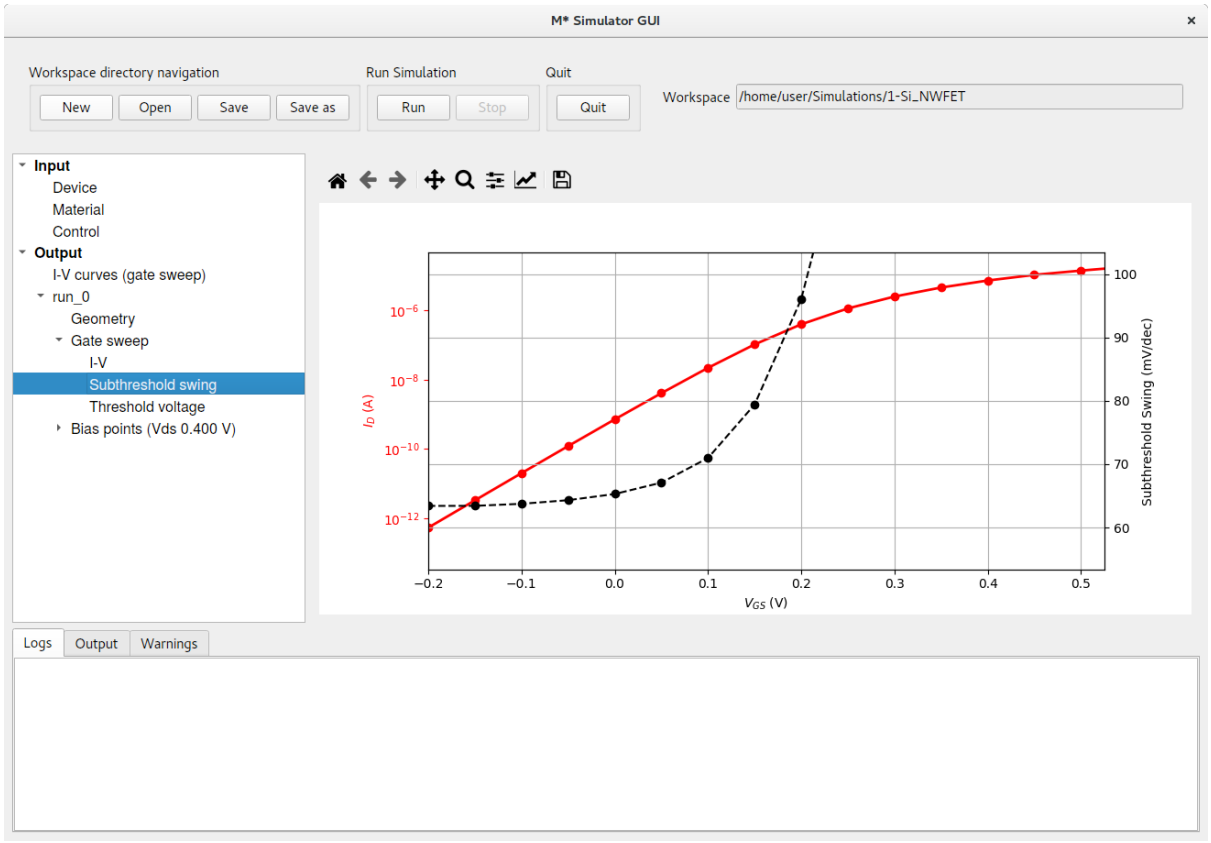


Figure 7: Subthreshold swing's dependence with gate bias. This device exhibits values below 70 mV/dec for gate voltages below 0.1 V.

– **Subthreshold swing** select this item to display a plot showing the $I_D - V_{GS}$ characteristics (semilogarithmic, left vertical axis) and the subthreshold swing computed at each gate bias. As shown below in fig. 7, this device exhibits excellent characteristics with a subthreshold swing below 70 mV/dec for gate voltages below 0.1 V

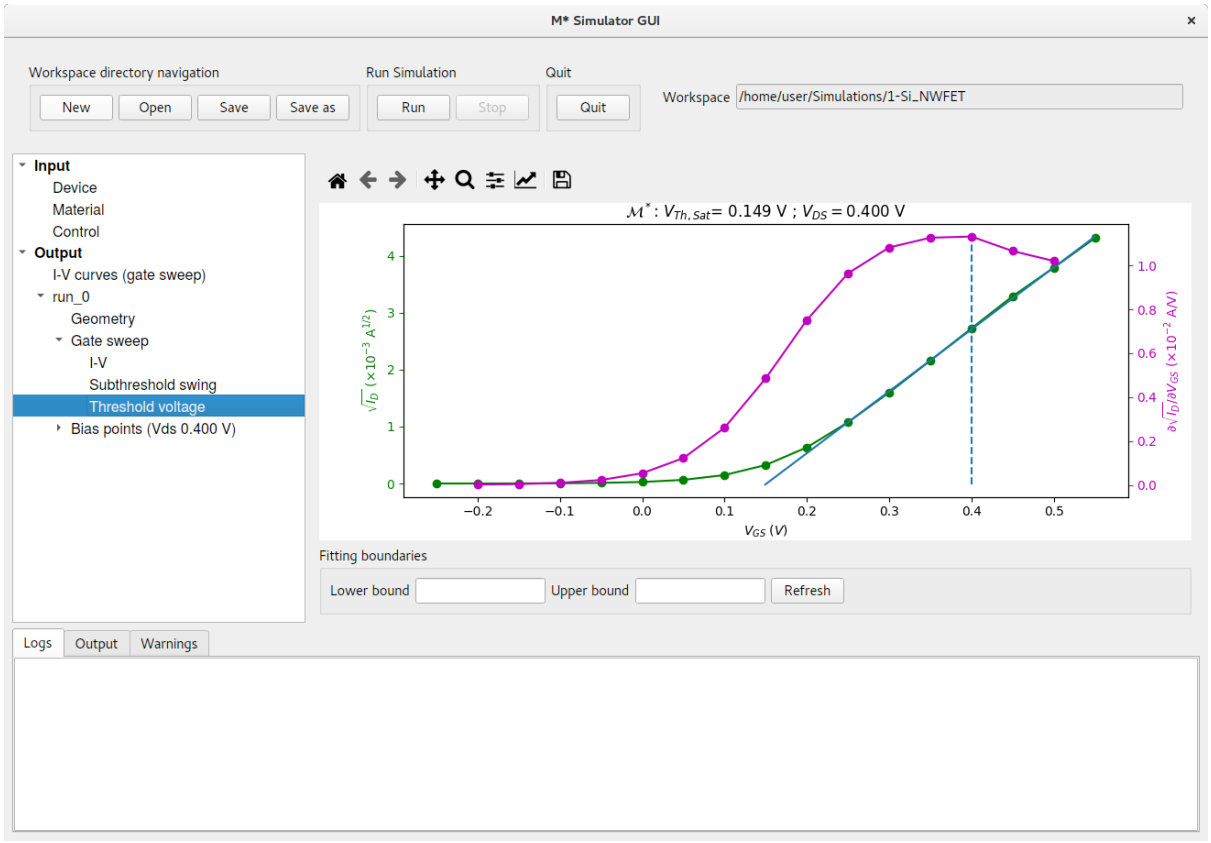


Figure 8: The device's threshold voltage extracted using the linear extrapolation method.

– **Threshold voltage** lists all gate bias sweep runs detected in your simulation folder, similar to the previous item in this list. Click on this item to display a plot illustrating the extraction of the device's threshold voltage using the linear interpolation method [1]. Two variations of the method will be employed depending on whether the device is considered to be operating in its linear region ($V_{DS} < 0.1$ V) or in its saturation region ($V_{DS} \geq 0.1$ V). The computed threshold bias is the value of $V_{GS}$ at which the blue line intersects the origin of the vertical left axis (shown in green). The blue line is computed using the slope of the green curve at the point where the magenta curve reaches its maximum value; indicated with a dashed vertical line (see fig. 8)

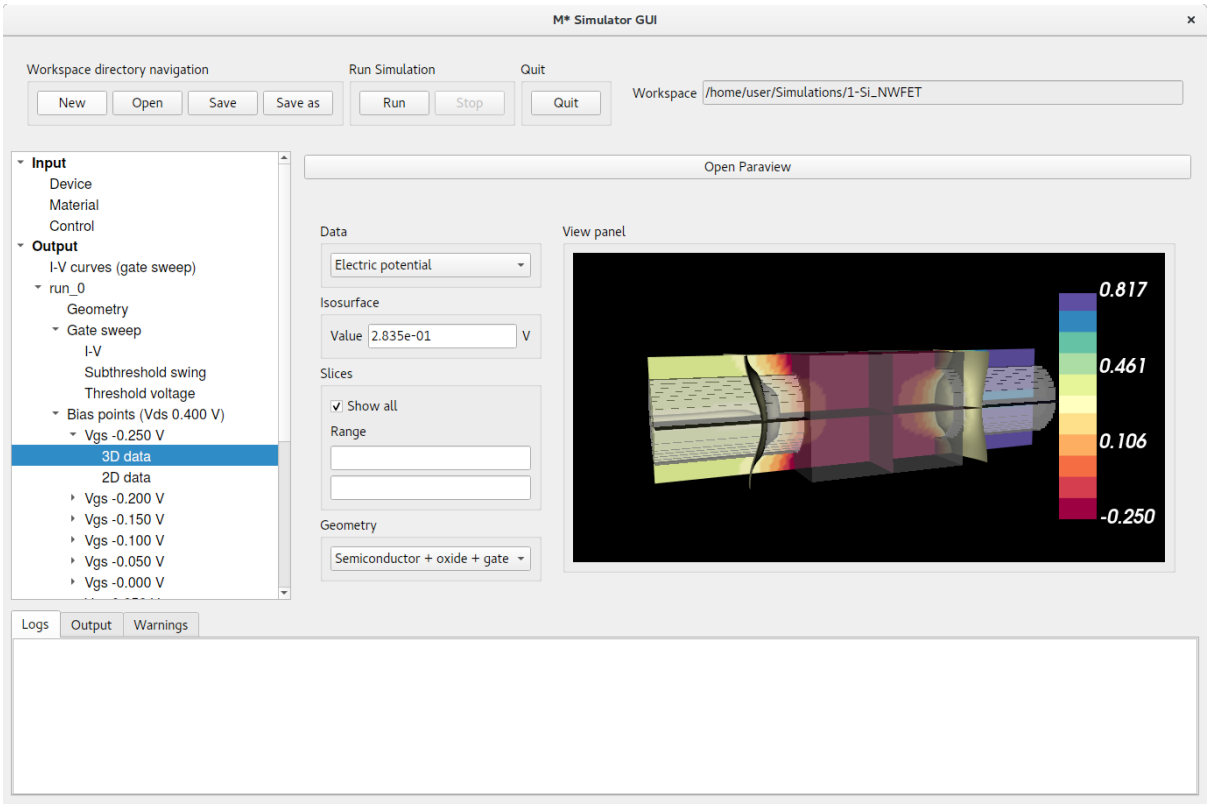


Figure 9: `3D data` panel displaying electric potential data with the device's geometry overlaid.

- **Bias points (Vds 0.400 V)** lists all bias points for which output data has been saved to disk. Expand this item to list gate voltages included in the present run –for which drain voltage has been kept to `Vds 0.400 V`–; expanding items associated with each gate voltage will reveal two sub-items:

  – `3D Data`: allows visualising the electric potential or carrier density on 3D grids. Select this item to show a 3D render of the electric potential with a semitransparent device geometry overlaid (fig. 9). The render will show an isosurface for the value input in the corresponding field while contour plots for slices along each cartesian axis are displayed upon ticking `Slices - Show all`; the limits of the colourmap can be manually set using the `Range` field. Displaying various elements of the device geometry can be controlled via the `Geometry` dropdown menu. You may select `Carrier density` in the `Data` dropdown menu to display a 3D render of that quantity instead, with similar controls available (fig. 10). Clicking the `Open Paraview` button at the top of this panel will display the 3D data in `ParaView`, a software package which allows further manipulation and visualisation options should you require so. We refer the reader to their user manual for further information [2, 3]

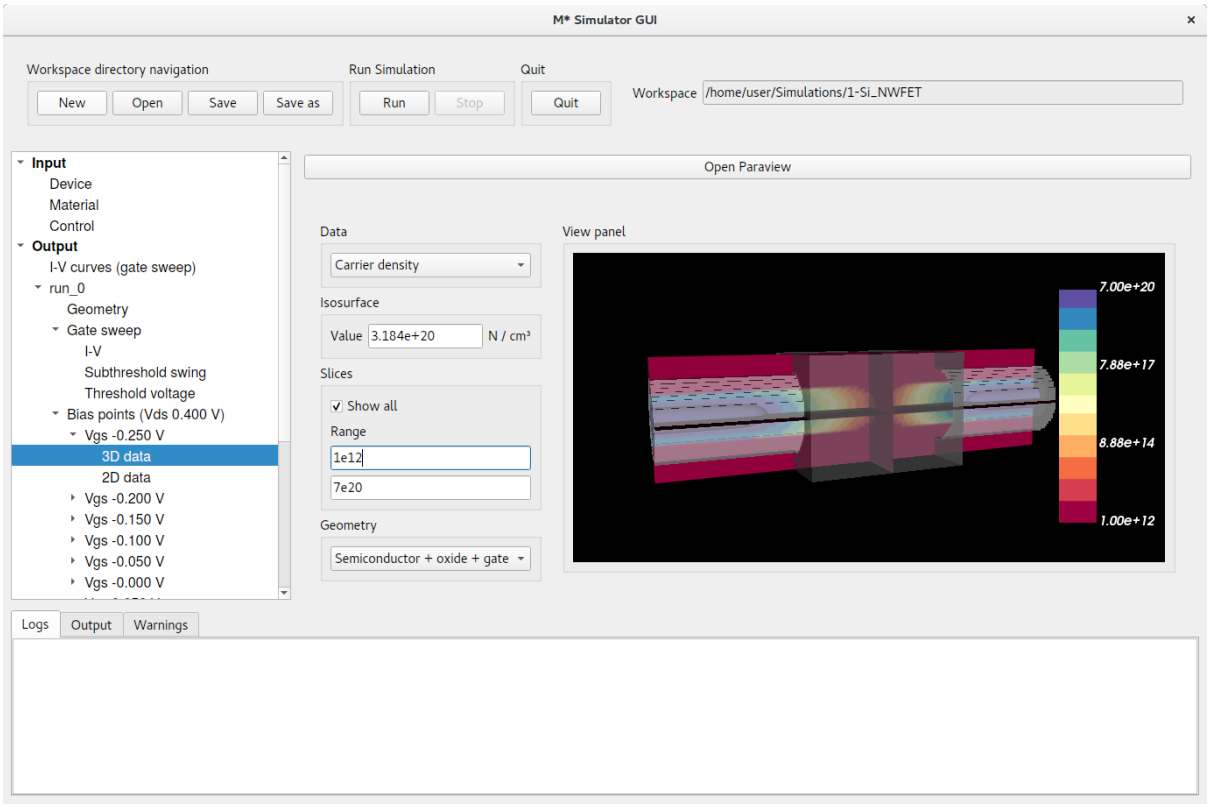


Figure 10: `3D data` panel displaying carrier density data with the device's geometry overlaid. Note the limits of the colourmap have been manually set using the `Range` fields.

– `2D data`: displays a contour plot of the local density of states (LDoS) and line plots indicating band edges for each valley. Additional quantities may be overlaid by ticking the corresponding tickboxes below the plot and clicking the `Refresh` button, as shown in fig. 11

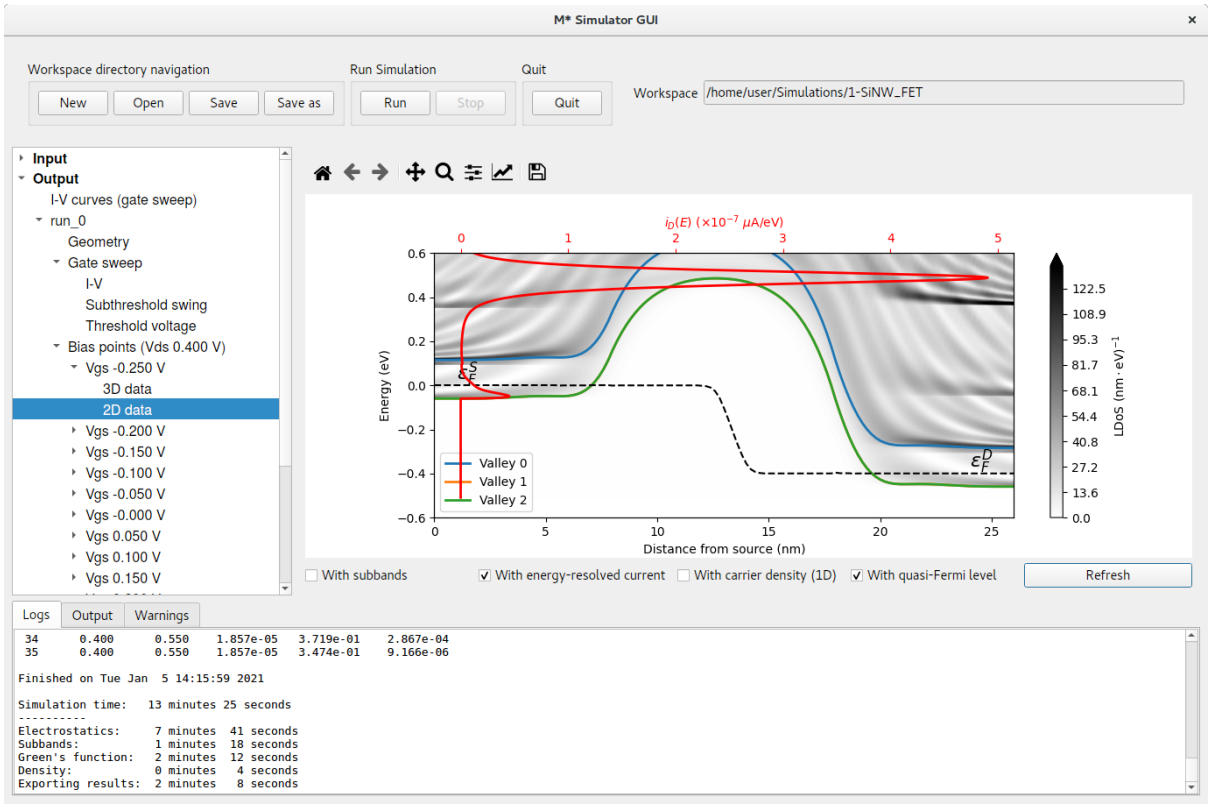


Figure 11: `2D data` panel displaying local density of states, energy-resolved current, and quasi-Fermi level data for an OFF state.

With these visualisation and post-processing tools you may study a device design's figures of merit, and their dependence with various geometrical, electrical, and material parameters. Let us now explore the effects of reducing the gate length from 10 nm to 5 nm on the threshold voltage and subthreshold swing by running a gate sweep simulation with appropriate modifications to the device geometry: Select `Input -> Device`, change the length of region 2 as shown in fig. 12 and click `Run`.

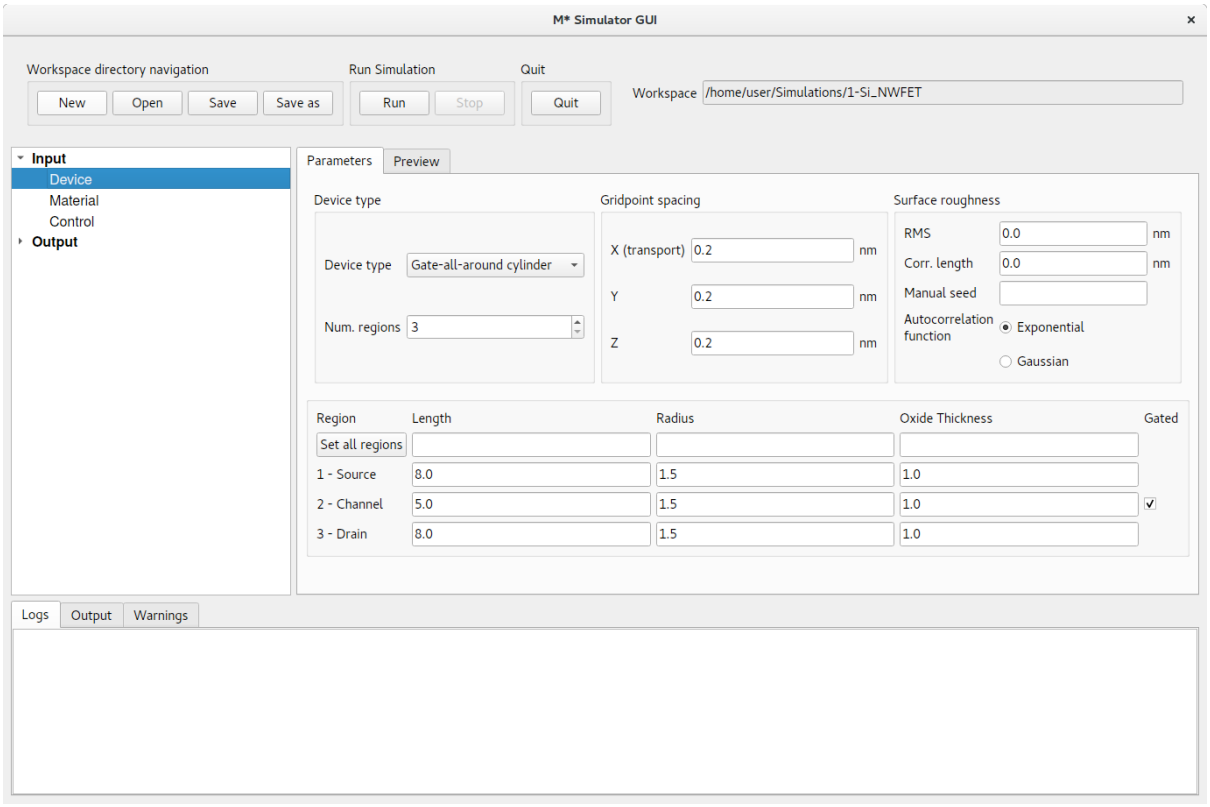


Figure 12: Reduce the length or region 2 from 10 nm to 5 nm in the `Input -> Device` panel and click `Run` to study the impact of reducing the device's channel length.

After this second simulation has completed, you will find its results listed under `Output->run_1` in the left pane, as shown in fig. 13. Note you can find all input and output data associated with each run in your workspace's subdirectories `run_0` and `run_1`. Navigate to the `Subthreshold swing` and `Threshold Voltage` panels of `run_1` to observe the impact of reducing the device's gate length in both quantities: the subthreshold swing degrades to values above 100 mV/dec (fig. 14), and the threshold voltage is reduced to approximately 30 mV in what is known as *threshold voltage roll-off* (fig. 14).

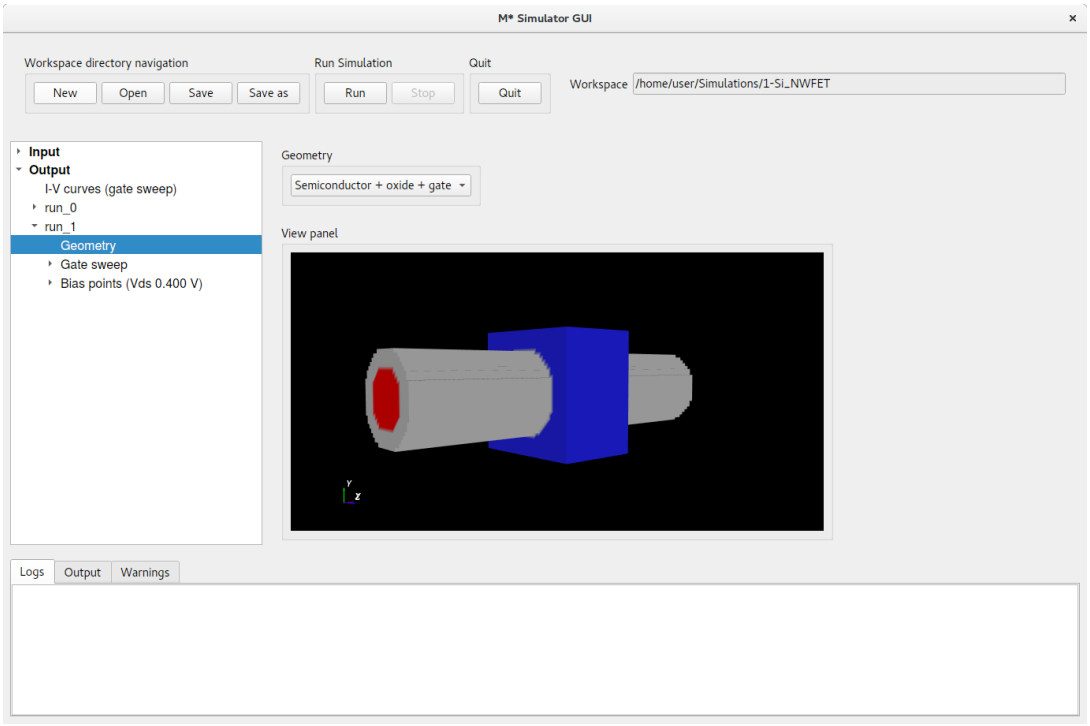


Figure 13: Once the second simulation with the reduced gate length finishes, you will find its output listed as `run_1`.

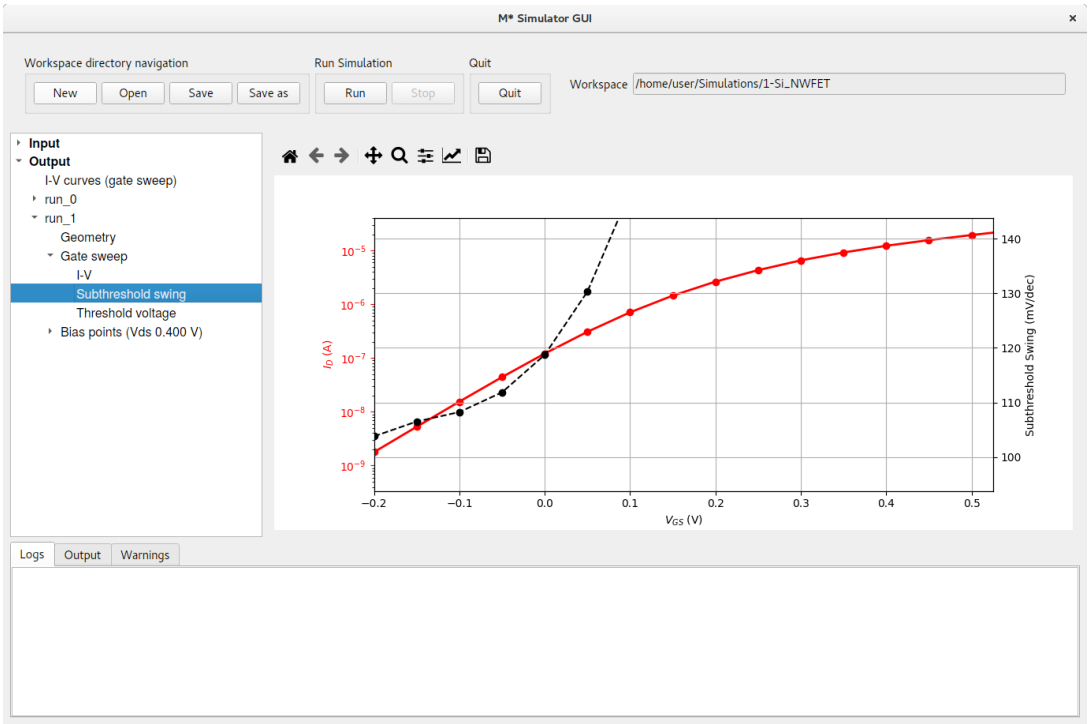


Figure 14: Reducing the device's gate length results in an increase of the subthreshold swing.

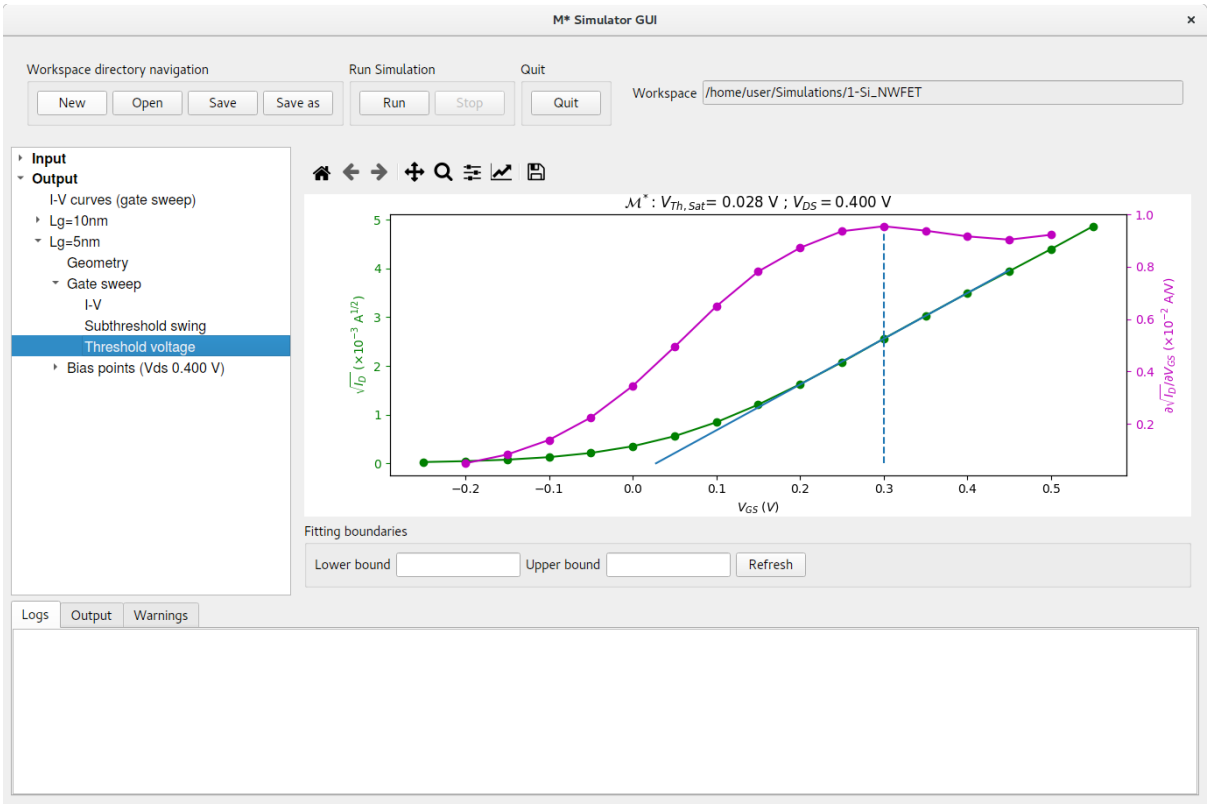


Figure 15: Reducing the device's gate length results in a shift of the threshold voltage towards a lower gate bias. Note simulations listed on the left pane have been renamed to more descriptive names, as discussed in section 1.1

## 1.1 Renaming simulations

By default, your simulations are labelled using the sequence `run_0`, `run_1`, `run_2`, etc. You may relabel them to something more convenient by either double-clicking their label or selecting the label on the left pane and pressing `F2` on your keyboard, and typing a new label. The corresponding subfolder within your workspace will be renamed accordingly.

To facilitate identifying runs performed so far let us rename `run_0` to `Lg=10nm` and `run_1` to `Lg=5nm`, as shown in fig. 15.

## 1.2 Comparing gate sweeps

We may directly explore the effects of reducing the device's gate length on its transfer characteristics using the `Output->I-V curves (gate sweep)` panel, as shown in ??. You may select which runs to include in the plot by activating the corresponding tick boxes on the list and clicking the `Refresh` button below.

Comparing data for both runs we can observe the aforementioned threshold voltage roll-off, as well as a significant increase in OFF currents when reducing the device's channel length. The latter can be attributed to increased source-to-drain tunnelling observed in the shorter channel device's OFF states, as evidenced by the energy-resolved current (red curve) in fig. 17 where most electron transport is located at energies below the channel's

band edge. This can be contrasted against the longer channel device's, where the largest contribution to OFF current occurs at energies above the channel's band edge (fig. 11).

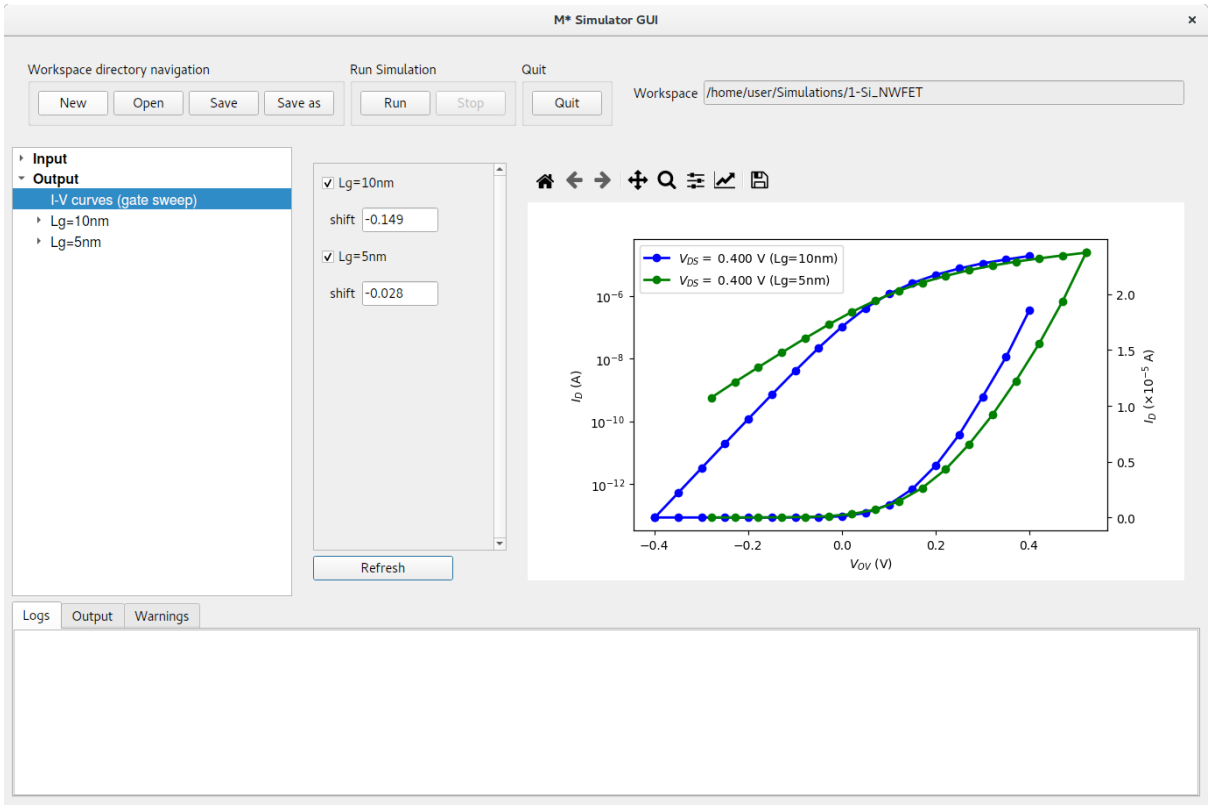


Figure 16: The `Output->I-V curves (gate sweep)` panel allows shifting curves along the horizontal axis for more meaningful comparisons. The horizontal axis' label has been manually set to $V_{OV}$ using the toolbar at the top of the plot.

In order to make this comparison more meaningful, let us shift their $I_D - V_{GS}$ characteristics by their respective threshold voltages to represent the overdrive voltage along the horizontal axis: $V_{OV} = V_{GS} - V_{Th}$. To do so, type each device's $-V_{Th,Sat}$ (with opposite sign) into their corresponding `shift` fields to align their threshold voltage with the horizontal axis' origin. Click `Refresh` to generate a plot similar to fig. 16. The horizontal axis' label has been manually set to $V_{OV}$ using the toolbar at the top of the plot.

An additional feature becomes apparent after shifting both curves: the device with shorter gate length exhibits decreased ON current when compared to the device with $L_G = 10$ nm at the same overdrive voltage. This is a consequence of larger tunnelling contributions to ON current in the shorter device, as can be seen in fig. 18.

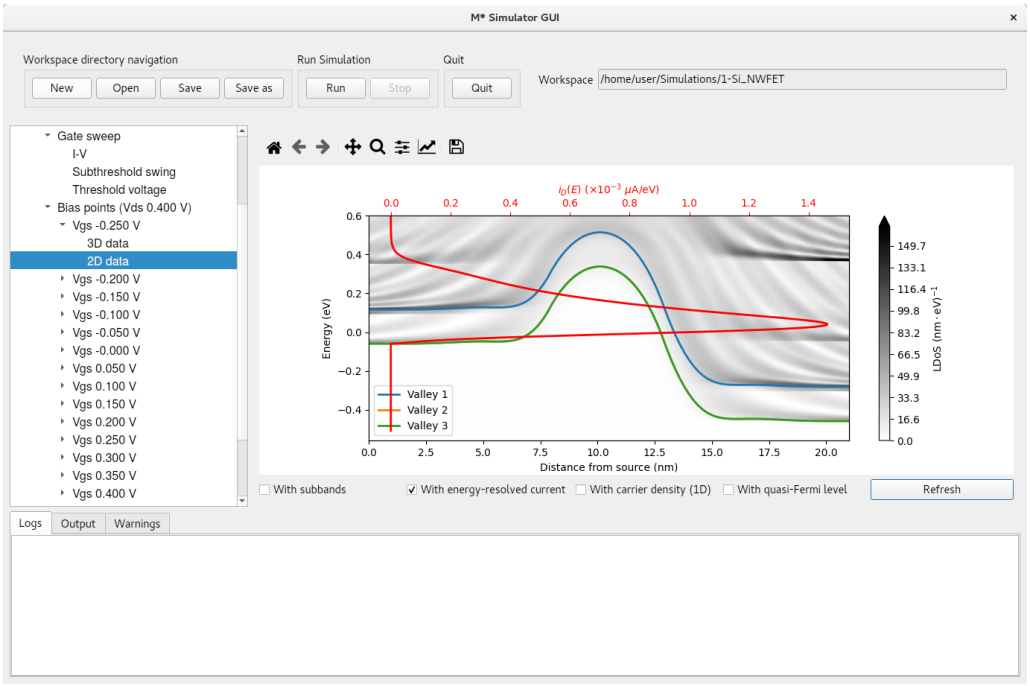


Figure 17: The shorter channel length device's 2D data reveals a stronger source-to-drain tunnelling contribution to OFF currents.

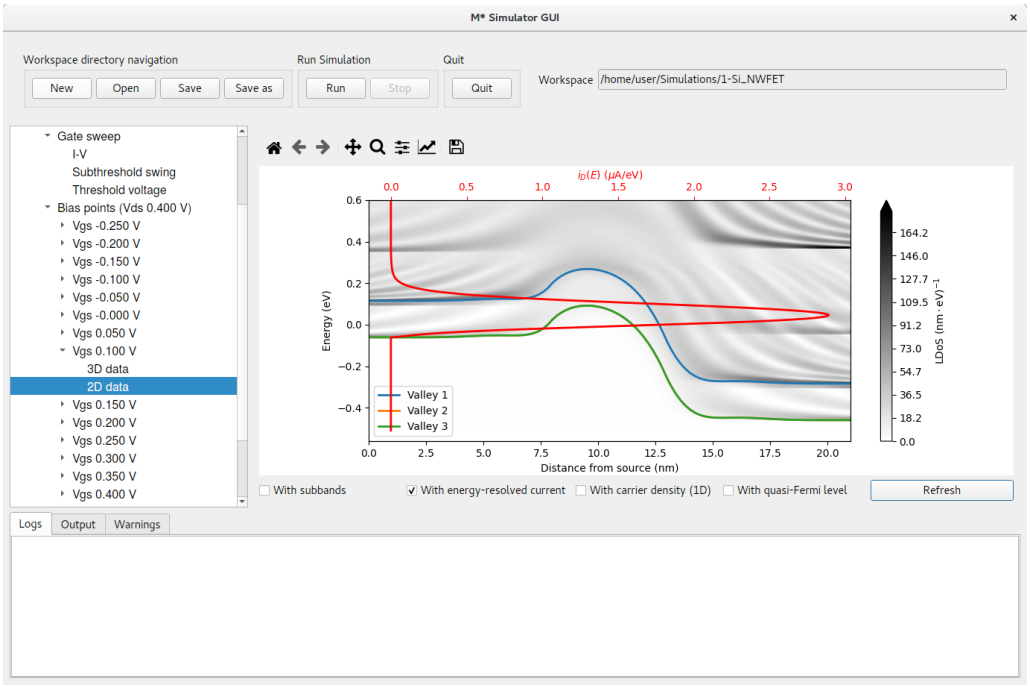


Figure 18: The shorter channel length device's 2D data reveals a strong source-to-drain tunnelling contribution to ON currents.

## 1.3 Drain sweeps

We continue by exploring the case of simulating a family of drain current curves by computing $I_D - V_{DS}$ characteristics at three different gate voltages. Select `Input -> Control` on the left pane and modify the `Voltage` section as (see fig. 19):

- `Gate voltage`: start by simulating a curve with a gate voltage of 0.2 V
- `Drain voltage`: set the starting drain voltage to 0.0 V
- `Iterate over`: select `Drain` from the dropdown menu
- `Voltage limit`: set the maximum drain voltage in your sweep to 0.4 V
- `Voltage stepsize`: leave this value set to 0.05 V

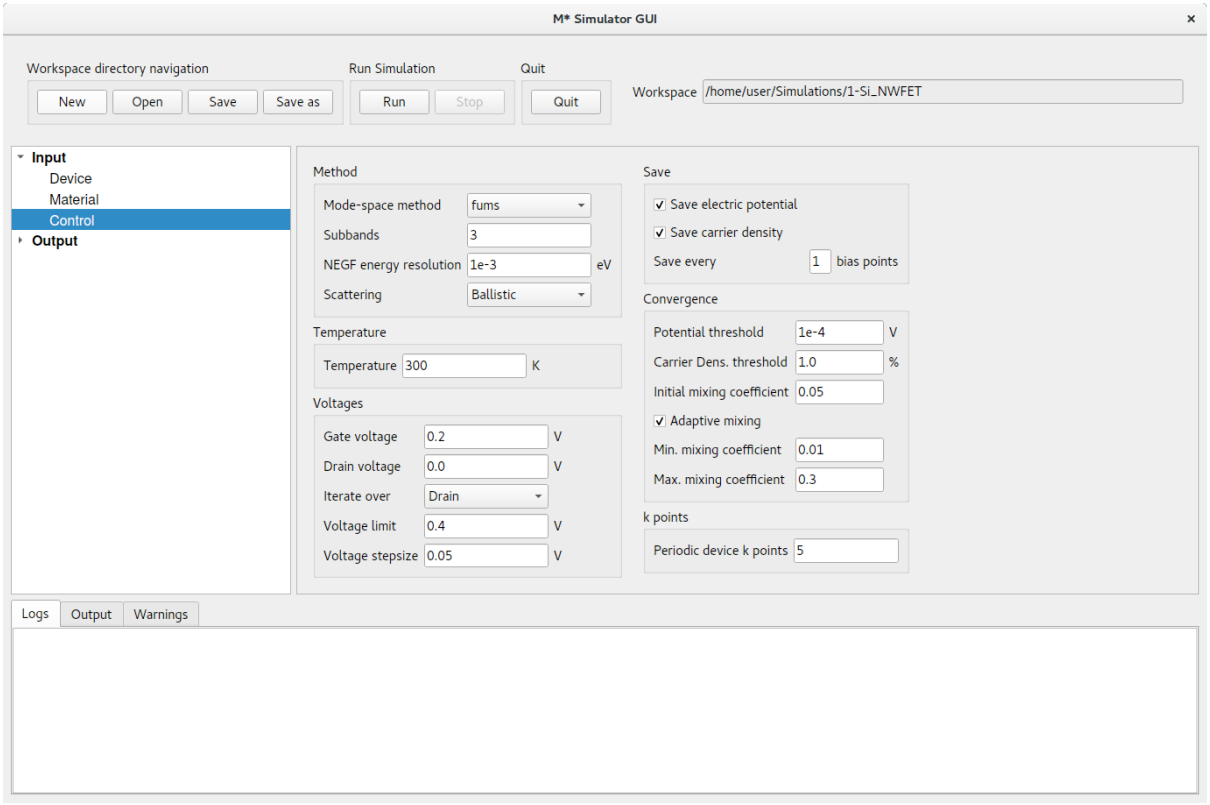


Figure 19: Modify the `Input->Control` panel to set up a drain sweep simulation.

Press the `Run` button to begin the simulation. Upon completion, results will be available at `Output->run_2` and corresponding data will be saved to a subdirectory named `run_2` within your workspace directory. Additionally, a new item will be listed under `Output` labelled `I-V curves (drain sweep)`; select it to display a plot of the device's $I_D - V_{DS}$ characteristics, as shown in fig. 20.

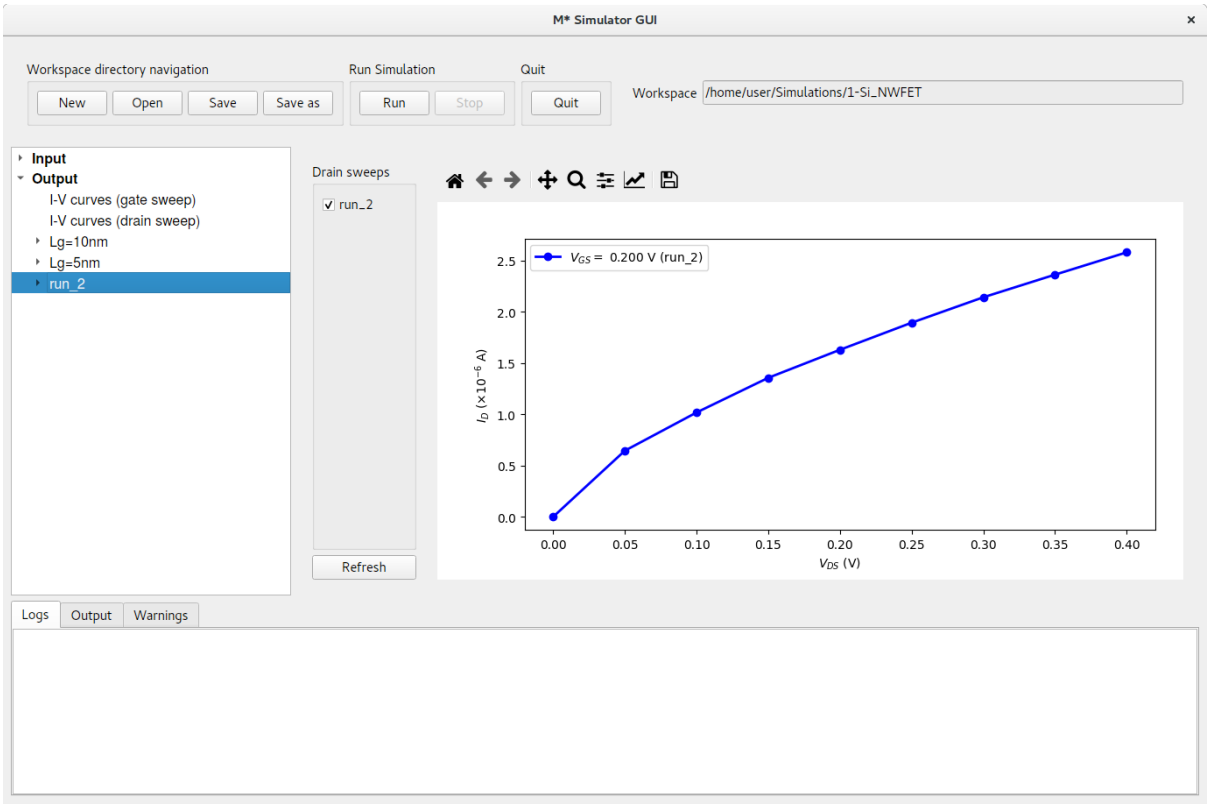


Figure 20: The `I-V curves (drain sweep)` panel allows visualising $I_D - V_{DS}$ characteristics.

To finalise this first tutorial, we shall illustrate how to visualise a family of drain curves using simulations performed at three different gate voltages: compute the two additional curves by increasing the value of `Gate voltage` to 0.3 V in the `Input->Control` panel and clicking `Run`; once this simulation has completed, perform one last simulation with a value of `Gate voltage` of 0.4 V. This process will generate `run_3` and `run_4`, which will be listed in the left pane's `Output` section. Select `Output->I-V curves (drain sweep)` now to visualise the results of the last three simulations in a single plot, as shown in fig. 21. You may use the tickboxes shown left of the plot to select which curves you wish to plot and click the `Refresh` button to update the plot.

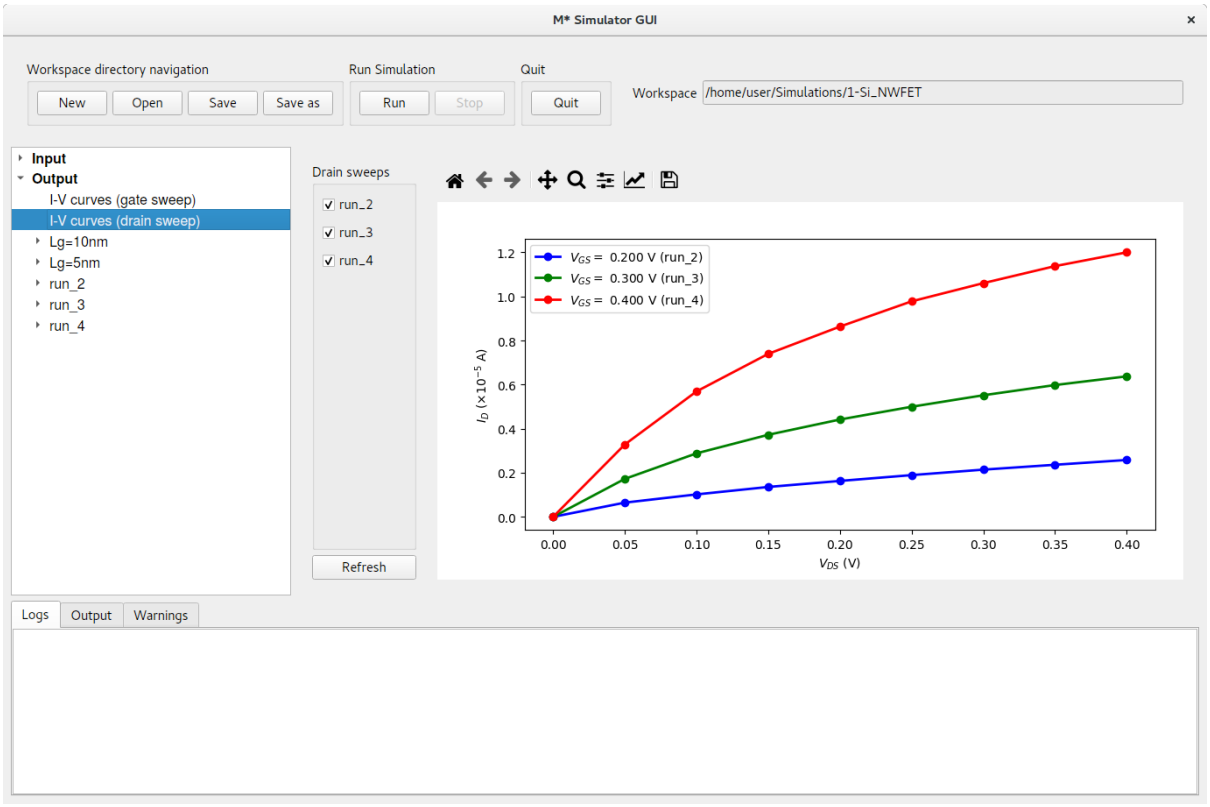


Figure 21: The `I-V curves (drain sweep)` panel allows comparing $I_D - V_{DS}$ characteristics from separate runs.

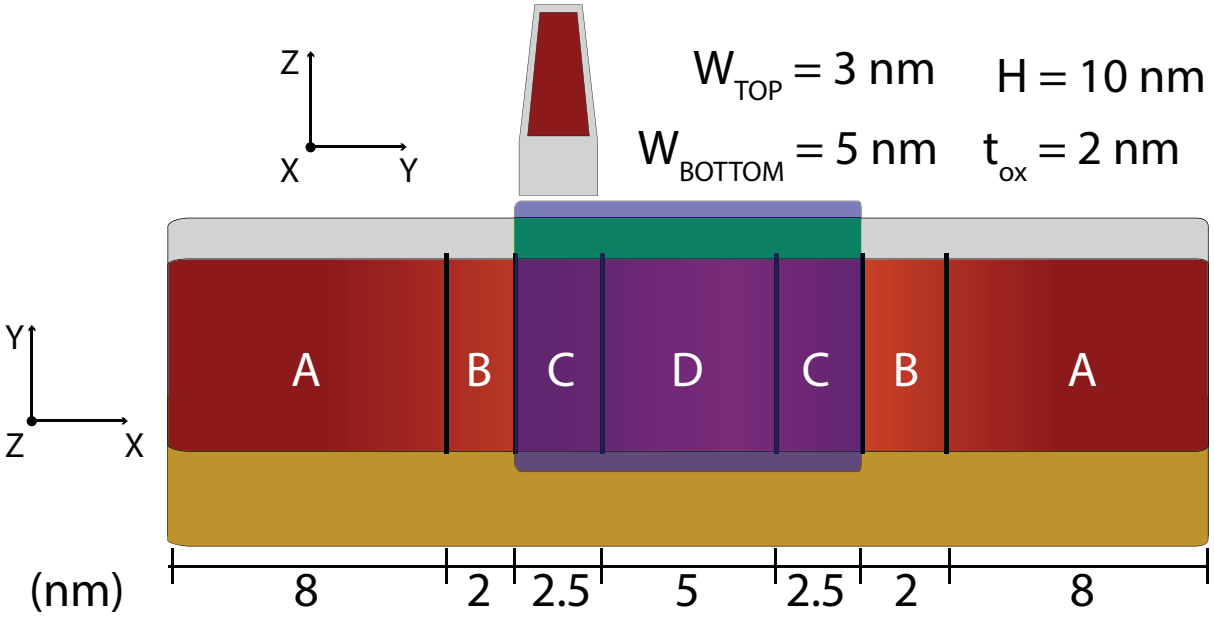


Figure 22: Ge FinFET: Schematic showing the device geometry. Red represents germanium, gray represents a low-$\kappa$ dielectric, green a high-$\kappa$ dielectric, yellow represents a silicon substrate, and blue the gate electrode. Regions in different shades of red represent variations in doping along the transport axis. The device is divided into several regions labelled A-D in order to describe dopant diffusion.

## 2 Tutorial: Germanium FinFET

In this tutorial we describe how to use $\mathcal{M}^*$ to simulate a germanium fin field-effect-transistor (FinFET) in a tri-gate configuration using the UMS mode-space method. The device is comprised of a Ge $\langle 100 \rangle$ fin with constant trapezoidal cross-section along the transport direction with a height of 10 nm, a width of 5 nm at the base of the fin, and a width of 3 nm at the top of the fin. Figure 22 shows a schematic of the device geometry and doping profile. The device is divided into 7 regions in which we target varying carrier densities in order to model dopant diffusion into the channel: regions labelled A in the figure are doped to target a carrier concentration of $1 \times 10^{20}$ cm$^{-3}$, regions labelled B to $5 \times 10^{19}$ cm$^{-3}$, regions labelled C to $1 \times 10^{18}$ cm$^{-3}$, and region D to $1 \times 10^{15}$ cm$^{-3}$.

In order to prepare the input files for simulating such a device, launch the $\mathcal{M}^*$ GUI and populate the three input panels as follows:

- **Device** select `Tri-gate fin` device type from the dropdown menu, set the number of regions to 7, and fill out the length of each region according to fig. 22 and as shown in fig. 23 below. Since this device's cross-sectional geometry is homogeneous, you may specify the corresponding fields for all regions at once by typing in values in the first row and clicking `Set all regions`. Set regions 3, 4, and 5 as `Gated`. Finally, set the `Gridpoint spacing` parameters to 0.2 nm $\times$ 0.33 nm $\times$ 1.0 nm to reduce simulation time. Before continuing, check the `Preview` tab to visualise your input geometry

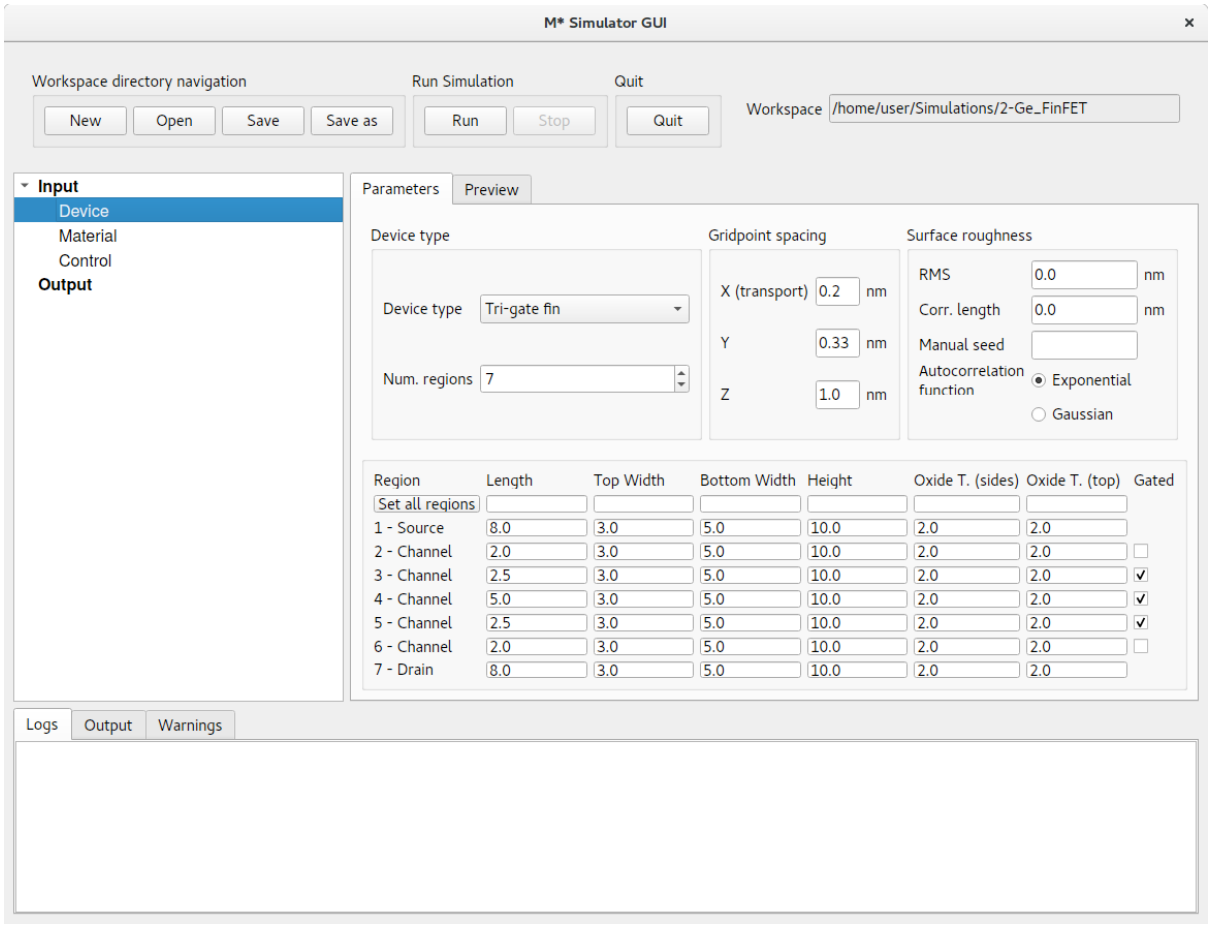


Figure 23: In the `Device` panel, set the device type to `Tri-gate fin` with 7 regions and dimensions shown above. Make sure only regions 3 - 5 are `Gated`. Increase the gridpoint spacing to reduce simulation time.

- **Material** set the material to `Ge, (010)/<100>, n-type` to set the semiconductor properties across the whole device. Cycle through regions 1 - 7 and set target carrier densities as described above for regions labelled A - D in fig. 22:
  - **A**: $1 \times 10^{20}$ cm$^{-3}$; $\varepsilon_r^{ox} = 4$
  - **B**: $5 \times 10^{19}$ cm$^{-3}$; $\varepsilon_r^{ox} = 4$
  - **C**: $1 \times 10^{18}$ cm$^{-3}$; $\varepsilon_r^{ox} = 20$
  - **D**: $1 \times 10^{15}$ cm$^{-3}$; $\varepsilon_r^{ox} = 20$

  Additionally, set the oxide permittivity to $\varepsilon_r^{ox} = 4$ to describe a low-$\kappa$ dielectric covering non-gated regions, and a value $\varepsilon_r^{ox} = 20$ in regions 3 - 5 to simulate a high-$\kappa$ oxide in gated regions. Set the buried oxide (BOX) permittivity to that of silicon (i.e. $\varepsilon_r^{box} = 11.7$) to simulate a device based on the aspect-ratio-trapping (ART) heteroepitaxy technique [4]

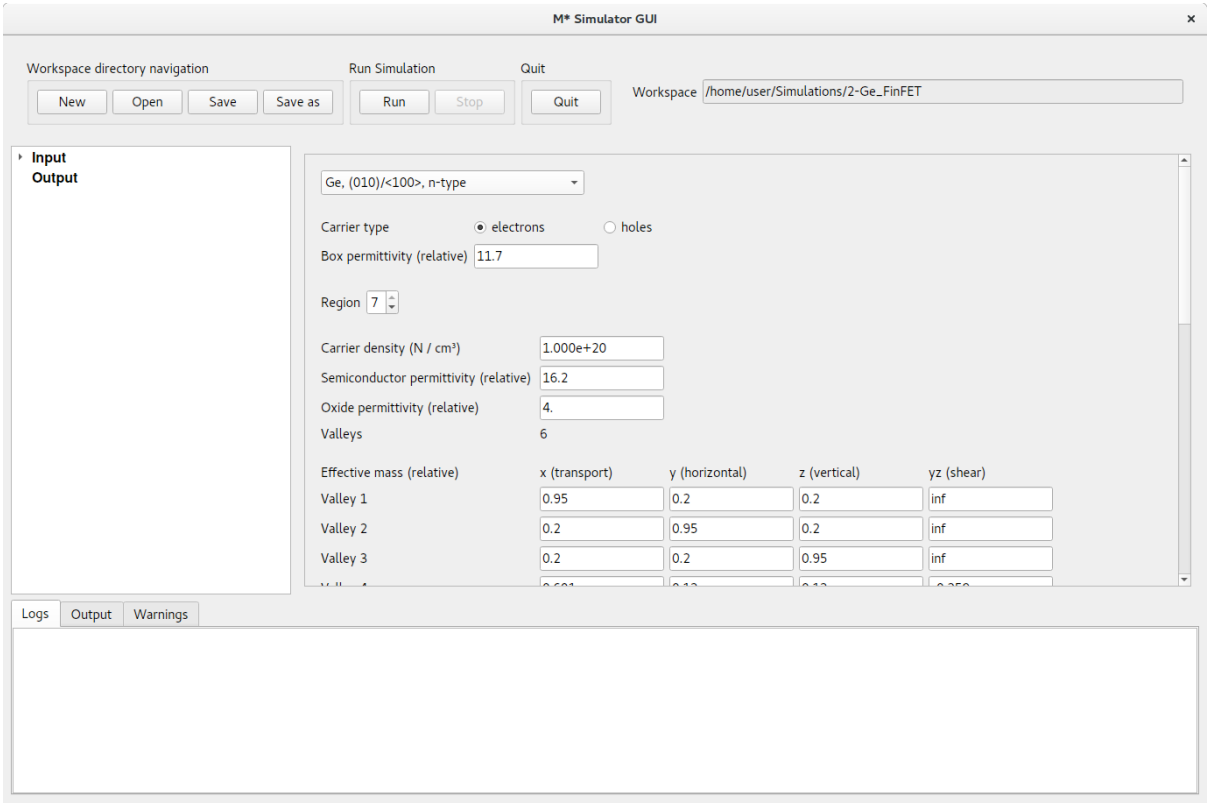


Figure 24: In the `Material` panel, cycle through regions to set the material properties discussed in the text above.

- **Control** set the mode-space method to UMS to explicitly solve the electronic structure at each slice along the transport direction for every iteration. Increase the number of subbands per valley to 10: devices with larger cross-sectional dimensions require larger values since weaker confinement effects result in smaller energy spacing between subbands. Set a gate voltage range of $[-0.4, 0.40]$ V by specifying those values for the `Gate voltage` and `Voltage limit` fields. Specify `Save` and `Convergence` variables as shown in fig. 25 below

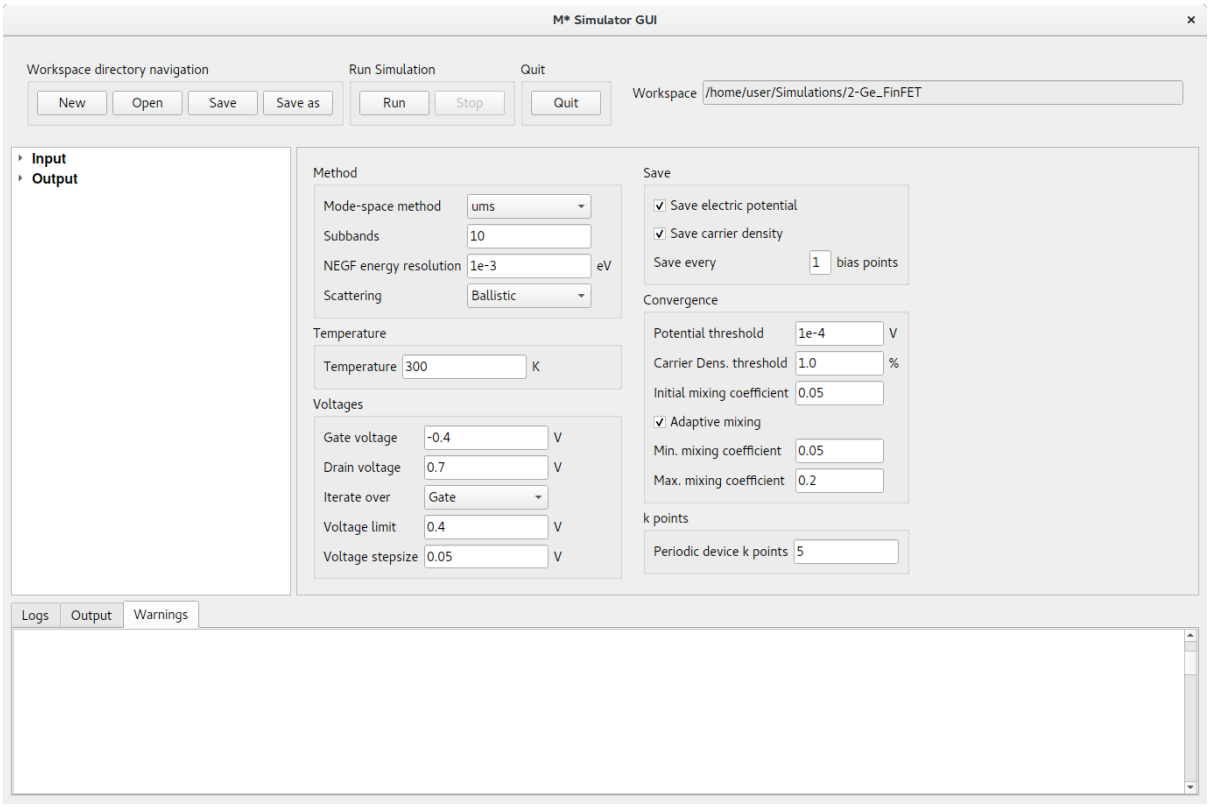


Figure 25: In the Control panel, select the mode-space method to UMS and set the number of subbands to 10. Fill out the rest of the fields with values shown.

Once you have entered and checked values, press the `Run` button to begin the simulation. After the first bias point has converged, you will see the first set of output data available under `Output->run_0`. Selecting `Geometry` brings up a 3D render similar to that shown in fig. 26. Note that although asymmetries can be observed in the semiconductor (red) - oxide (gray) interface as a result of the method employed for visualisation; the geometry grid employed in the simulation may not contain any asymmetries that could influence simulation results.

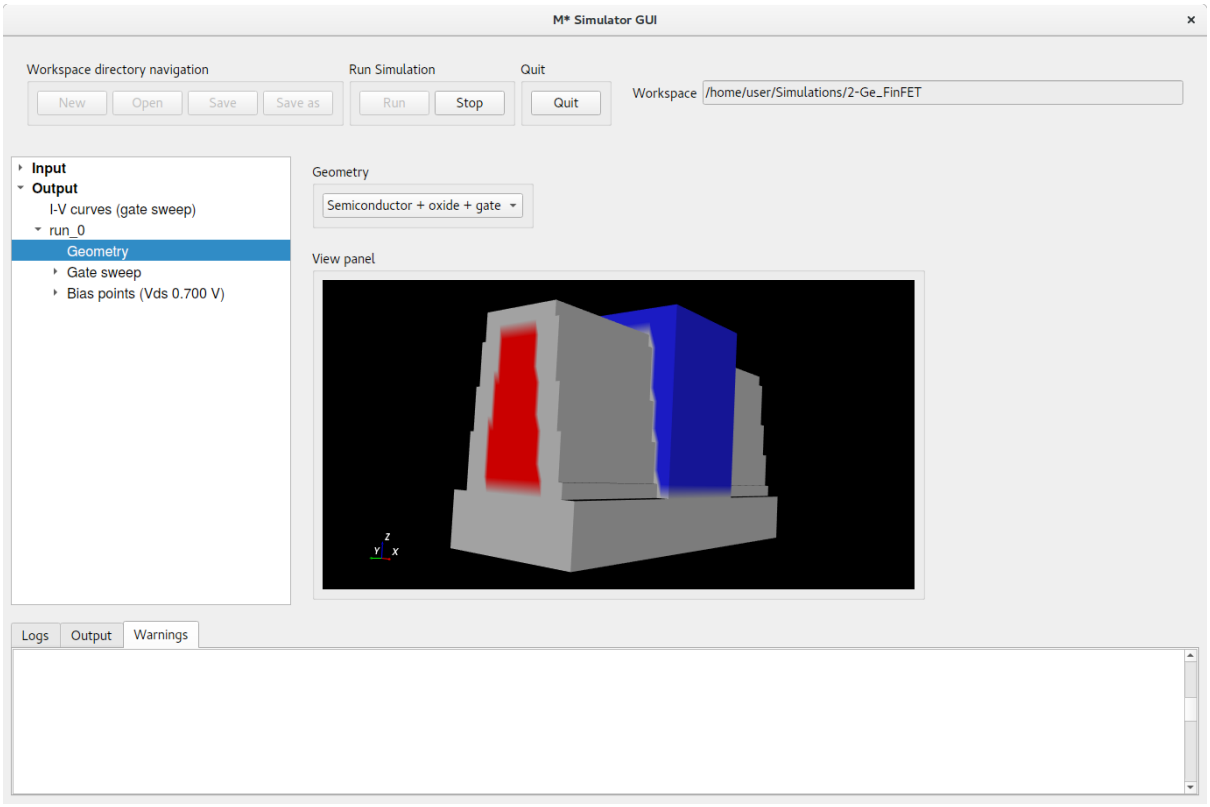


Figure 26: Geometry of the simulated Ge FinFET. Asymmetries observed in the semiconductor-oxide interface are a visualisation artifact and not a feature of the grid employed in the simulation.

Once the simulation has completed, you may visualise all quantities discussed in the previous tutorial such as $I_D - V_{GS}$ characteristics, subthreshold swing vs. gate voltage, etc. To plot the simulated dopant distribution plot the 2D data associated with an OFF state and include the 1D carrier density profile by activating the corresponding tickbox and clicking `Refresh`, as shown in fig. 27. Note the carrier density discontinuities occurring at the boundaries across regions.

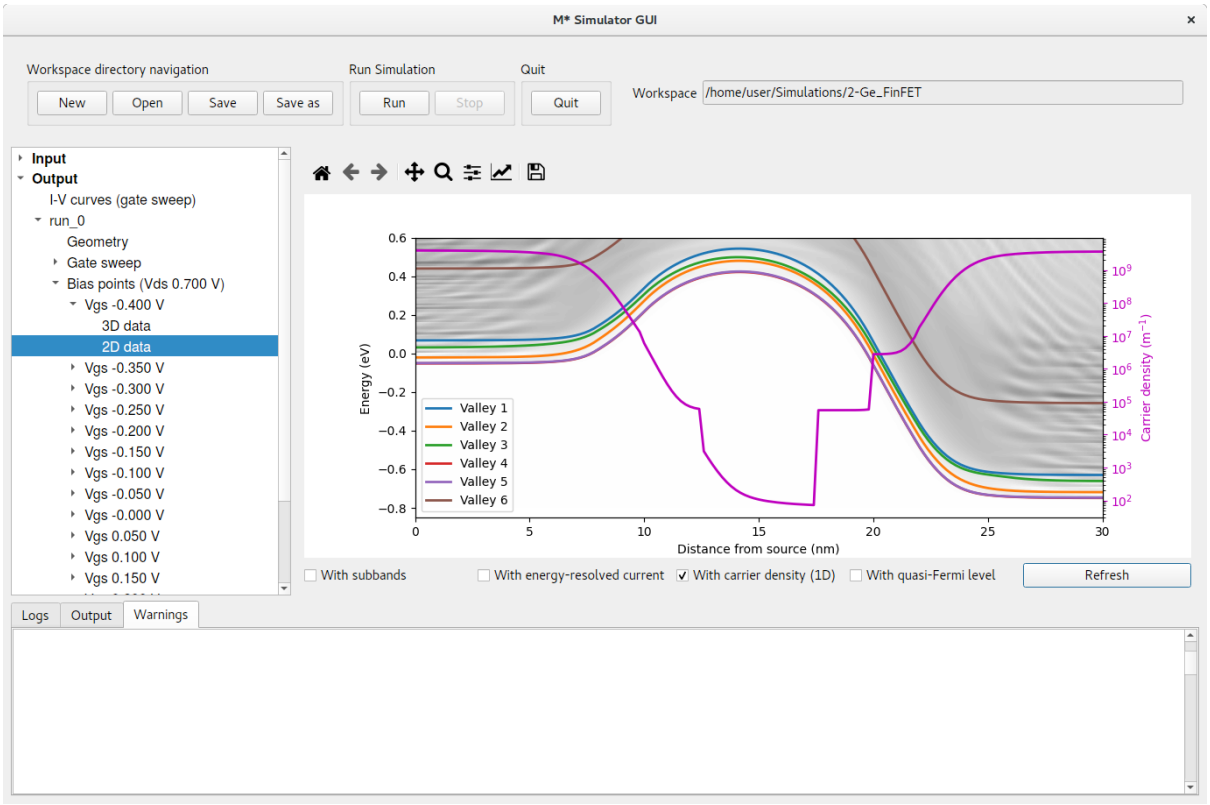


Figure 27: Local density of states and 1D carrier density profile for an OFF state.

Select the 2D data corresponding to an ON state to plot the associated local density of states and each valley's first subband; overlay both energy-resolved current and 1D carrier density profile to generate a figure similar to that shown in fig. 28. Note discontinuities in the 1D carrier density profile imposed by the doping profile have now been washed out by the larger carrier densities associated with ON states. From the energy-resolved current (red curve) and first subbands for each valley we can observe that `Valley 6` does not participate in transport and could be safely ignored in the simulation without altering results. This corresponds to the Γ valley, whose low effective mass (0.041) results in a large impact of quantum confinement effects and thus a significant shift towards higher energies, rendering it irrelevant for the transport properties of this nanoscale device.

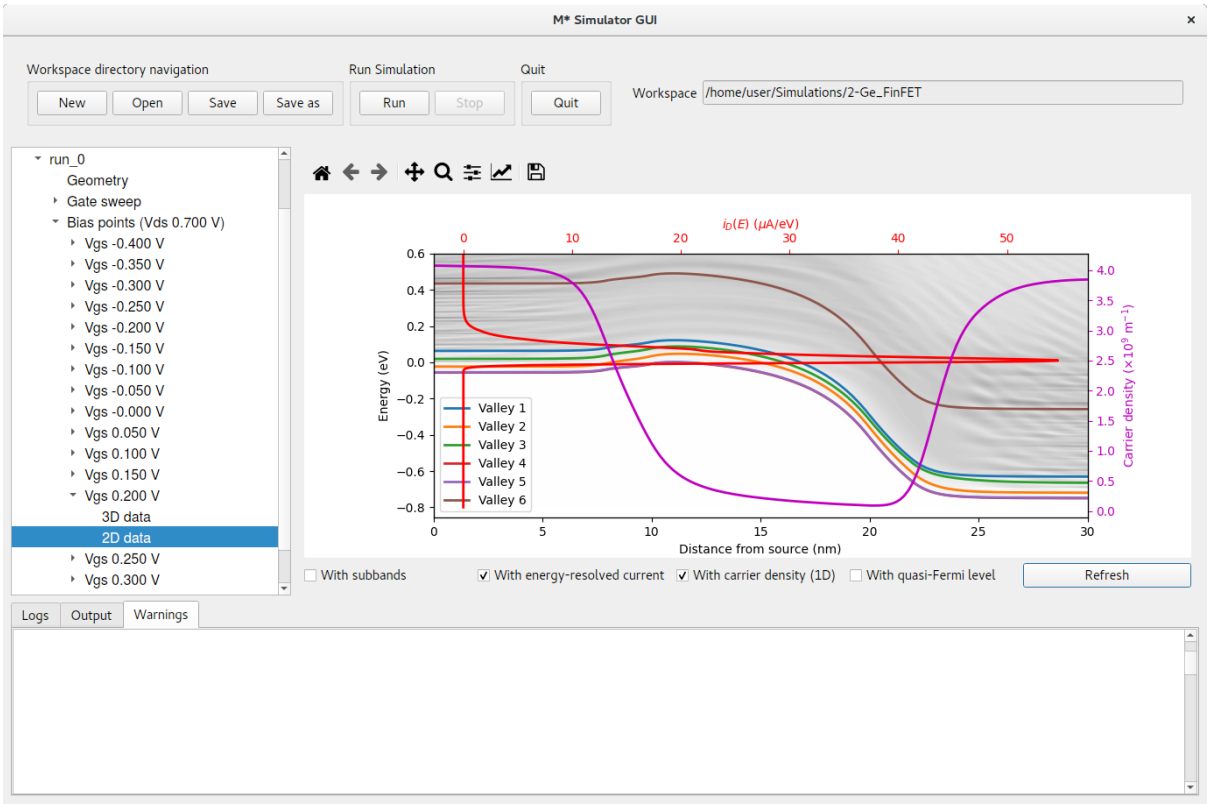


Figure 28: Local density of states, energy-resolved current, and 1D carrier density profile for an ON state.

Let us now inspect the shape of the electric potential and carrier density as the device turns ON; go into `Output->run_0->Gate sweep->Threshold voltage` to find an appropriate bias point to investigate.

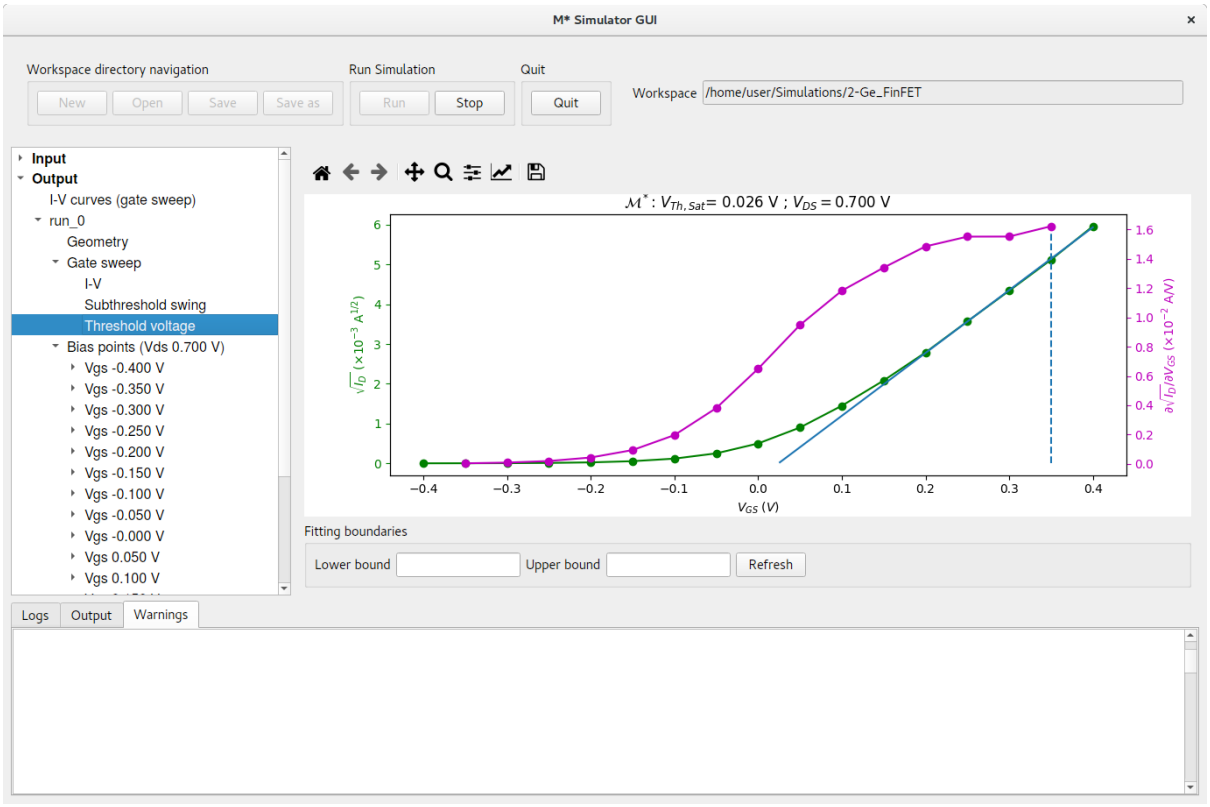


Figure 29: Threshold voltage extraction using the linear extrapolation method for saturation region of operation (i.e. large $V_{DS}$).

As shown in fig. 29, a value of $V_{Th,Sat}$ close to 0.050 V is found for this device. Visualise the 3D data output for $V_{GS} = 0.050$ V to inspect the electric potential and carrier density as the device turns on: asymmetries along the transport and height directions can be observed in both quantities as a result of the applied drain-source bias and trapezoidal cross-section, respectively. Note how the isosurfaces plotted in figs. 30 and 31 reveal charge carriers begin to flow from the bottom half of the fin as the device turns ON. You may confirm carrier density increases near the top of the fin for larger values of $V_{GS}$ by inspecting the 3D carrier density for higher ON states, as shown in fig. 32.

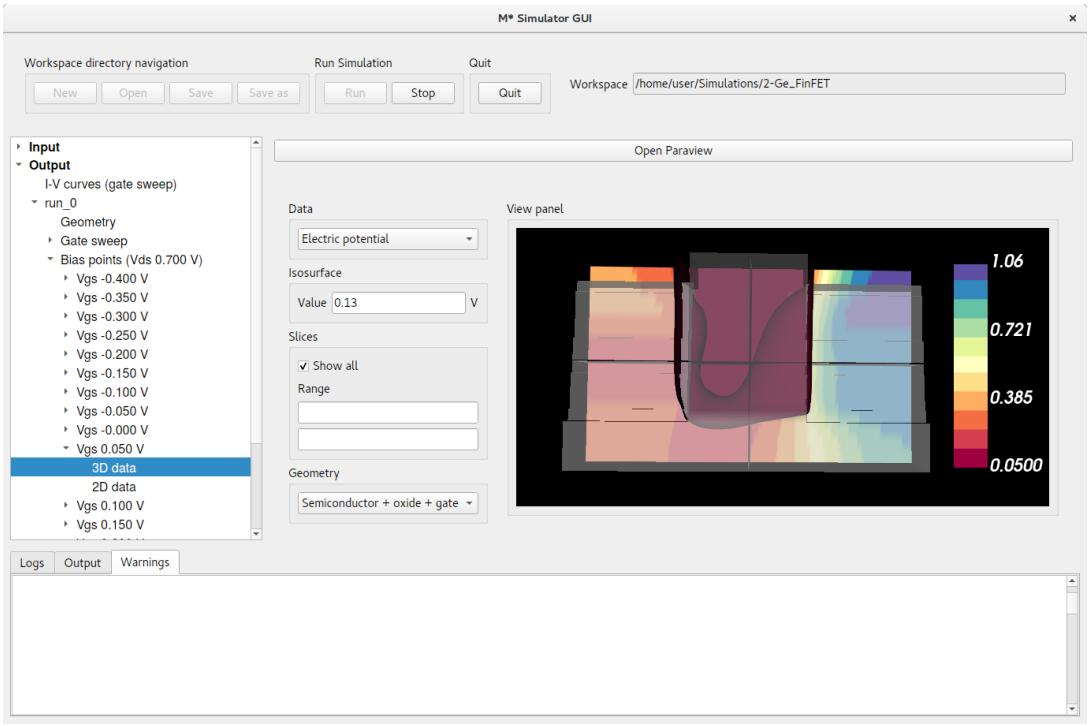


Figure 30: Electric potential around $V_{GS} = V_{Th,Sat}$.

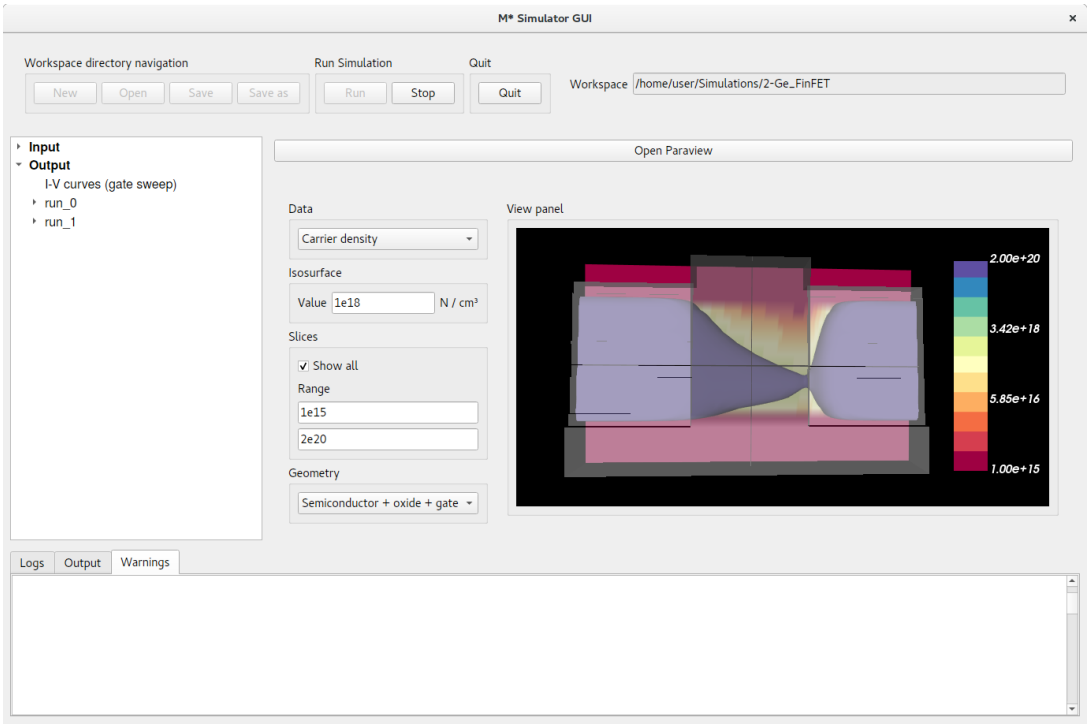


Figure 31: Carrier density around $V_{GS} = V_{Th,Sat}$. Shown isosurface corresponds to a carrier density of $10^{18}$ cm$^{-3}$.

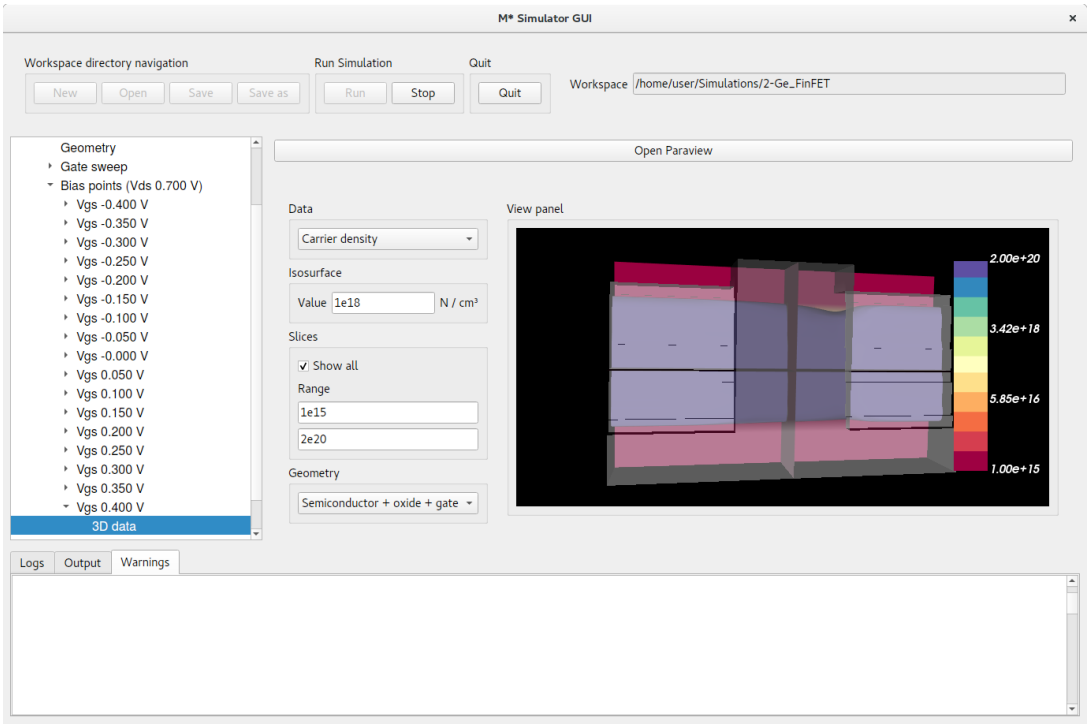


Figure 32: Carrier density when the device is in saturation region. Shown isosurface corresponds to a carrier density of $10^{18}$ cm$^{-3}$.

To finish this tutorial, we explore the effect of employing the fast uncoupled-mode space approximation for simulating this device's transfer characteristics. Select `Input->Control` in the left pane and change the mode-space method to FUMS while maintaining the same values for all other simulation parameters; click `Run` to begin the simulation. This simulation should be significantly faster. Once completed, you will find the corresponding output data listed in `Output->run_1`. Select `Output->I-V curves (gate sweep)` in the left pane to show a comparison of $I_D - V_{GS}$ curves simulated with UMS and FUMS, as shown in fig. 33. Note how slight differences can be observed in the semilogarithmic plot only for OFF states, while differences are only noticeable in the linear scale plot for ON states. This is a consequence of the fact that differences in computed current values differ significantly more in OFF states (up to $\approx 35\%$) than in ON states (up to $\approx 10\%$). You can confirm differences in other computed quantities such as subthreshold slope and threshold voltage are negligible, making FUMS an attractive alternative for simulating certain properties of small devices with by yielding satisfactory results at a lower computational cost.

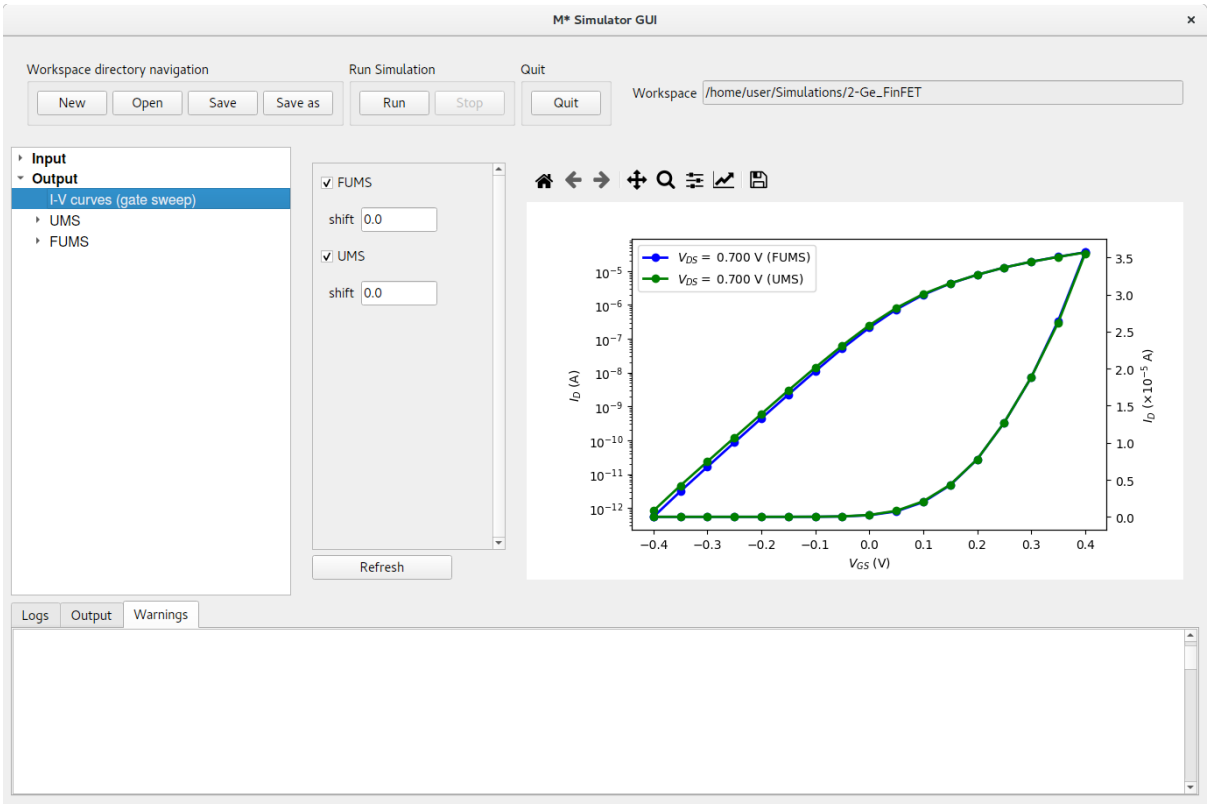


Figure 33: Transfer characteristics computed with UMS (`run_0`) and FUMS (`run_1`).

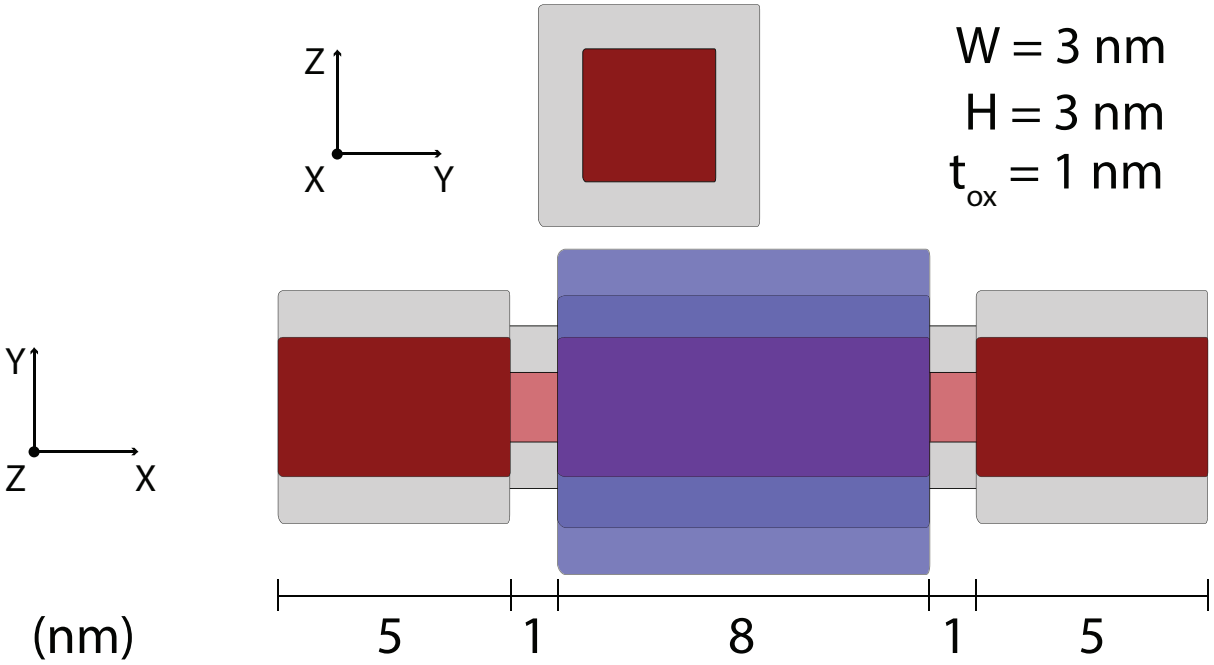


Figure 34: Si SET: Schematic showing the device geometry. Red represents silicon, gray represents silicon dioxide, and blue the gate electrode.

# 3 Tutorial: Silicon single-electron transistor (SET)

In this tutorial we illustrate $\mathcal{M}^*$'s capabilities for simulating the properties of devices whose operation inherently depends on quantum mechanical effects through a single-electron transistor design. The device is comprised of a Si nanowire with tunnelling barriers on either side of the channel realised via geometrical constrictions. This design is inspired by ref. [5] and shown schematically in fig. 34. To set up a simulation for this device, fill out the input panels as follows:

- **Device** select `Gate-all-around trapezoid` as the device type and enter geometrical parameters in accordance with fig. 34 and as shown below in fig. 35. Note that although we shall be simulating a device with a square cross-section, this device type allows variations in width between the top and bottom portions of the geometry. Once you have finished, check the geometry corresponds to the intended design by clicking on the `Preview` tab

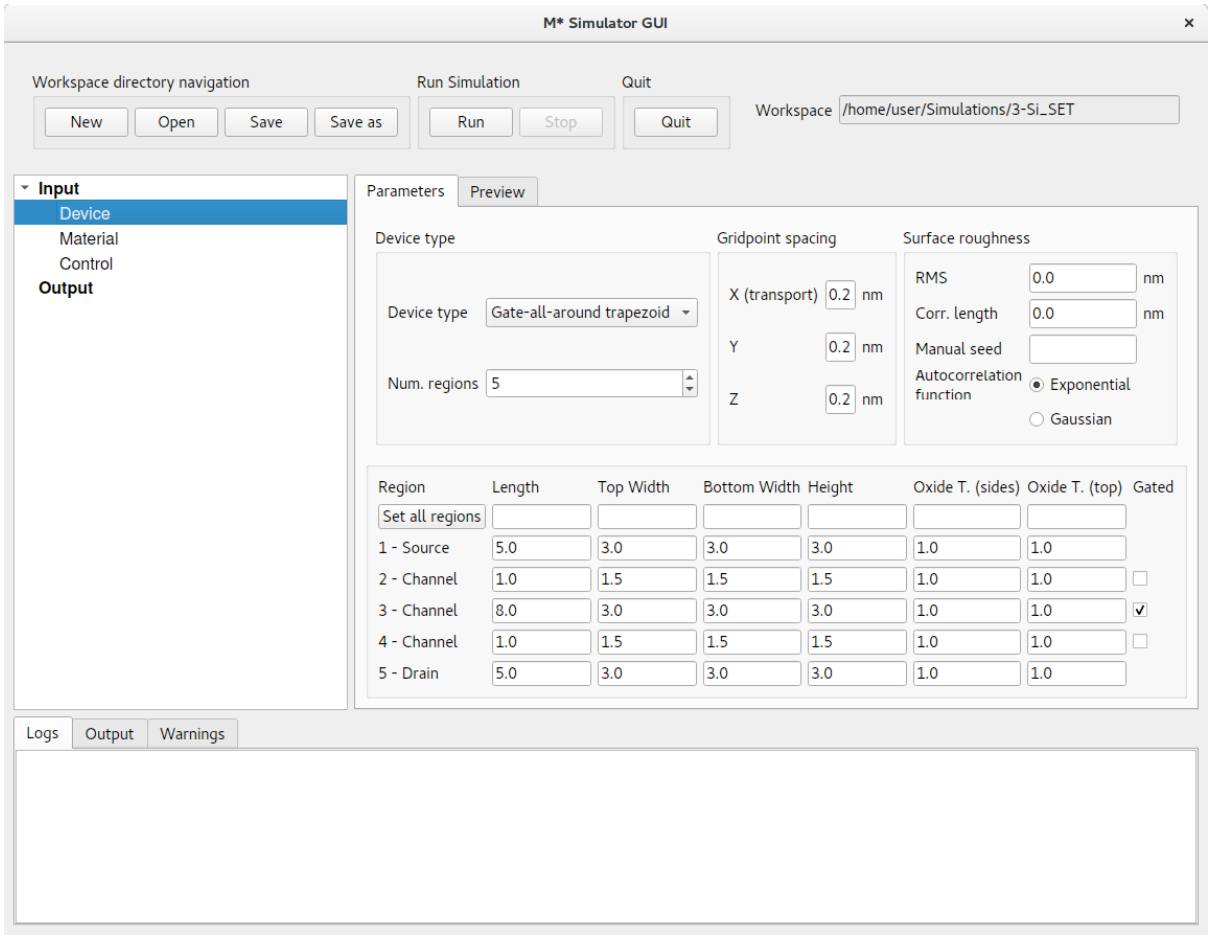


Figure 35: In the `Device` panel, specify a `Gate-all-around trapezoid` with 5 regions and dimensions shown above. Make sure only region 3 (i.e. the device channel) is `Gated`.

- **Material** select `Si, (010)/<100>, n-type` and cycle through regions to set a target carrier concentration of $2 \times 10^{20}$ cm$^{-3}$ in source and drain extensions (i.e. regions 1 & 5), and zero in regions 2 - 4. Leave the default oxide relative permittivity of $\varepsilon_r = 3.9$ corresponding to $SiO_2$

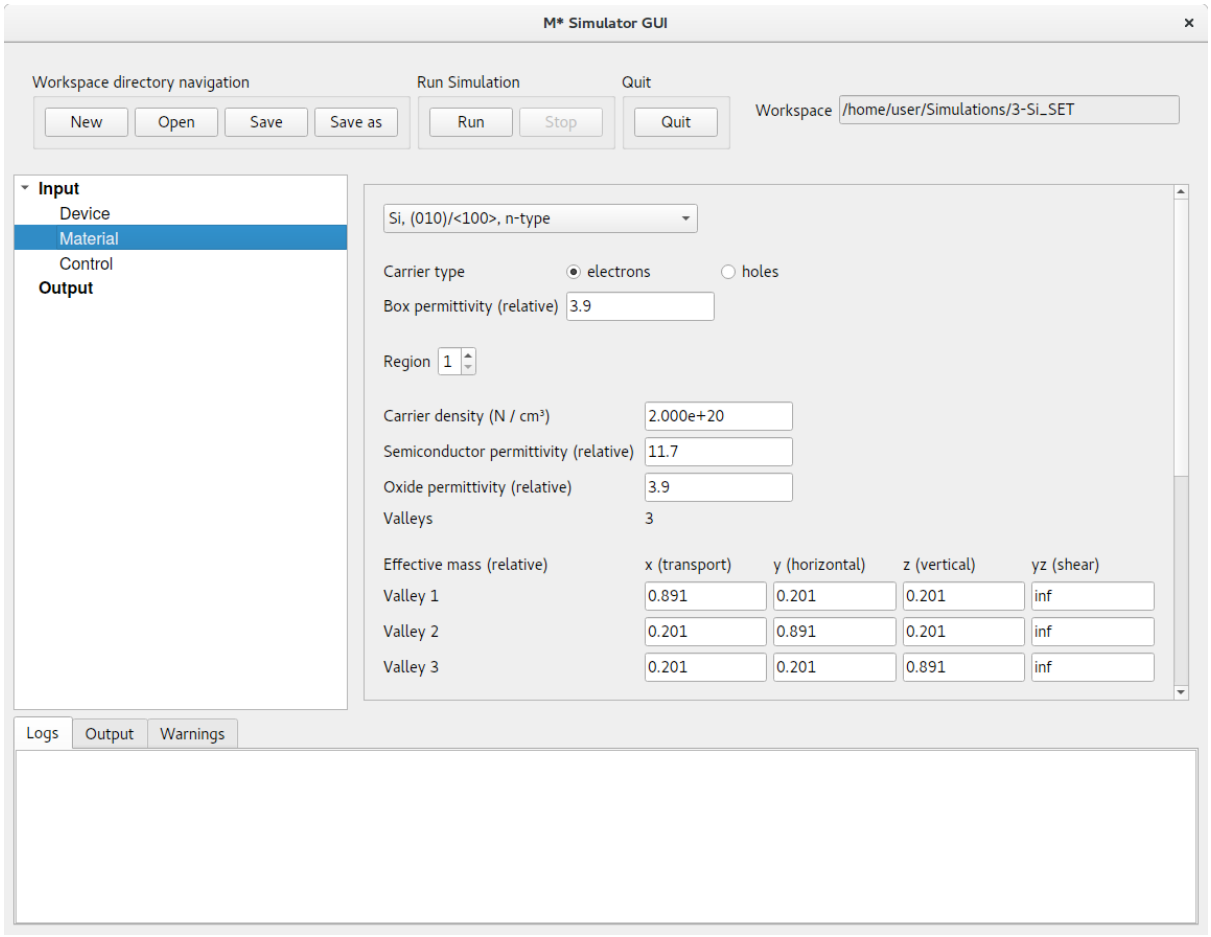


Figure 36: In the `Material` panel, specify a dopant concentration of $2 \times 10^{20}$ cm$^{-3}$ in both source and drain extensions and a value of zero for all regions in between.

- **Control** select coupled-mode space (CMS) as the mode-space method, as required for all devices with heterogeneous cross-sectional dimensions, and 4 subbands per valley. Since this device will exhibit strong state quantisation, we need to increase the resolution of the NEGF solver in order to capture states that are very narrow in energy; increase `NEGF energy resolution` to $10^{-4}$ eV to ensure an adequate description of the density of states throughout the device. Furthermore, set a temperature of 77 K and a drain voltage of 0.015 V for enhanced observation of quantum effects. A gate voltage sweep of $[0.0, 1.2]$ V in steps of 0.05 V is adequate to explore all regions of operation. Enable saving electric potentials and carrier densities, and set `Save every [2] bias points` to reduce disk space usage as saving data for every other bias point should provide enough data to study the device. Finally, set the same convergence parameters as in previous tutorials and shown in fig. 37

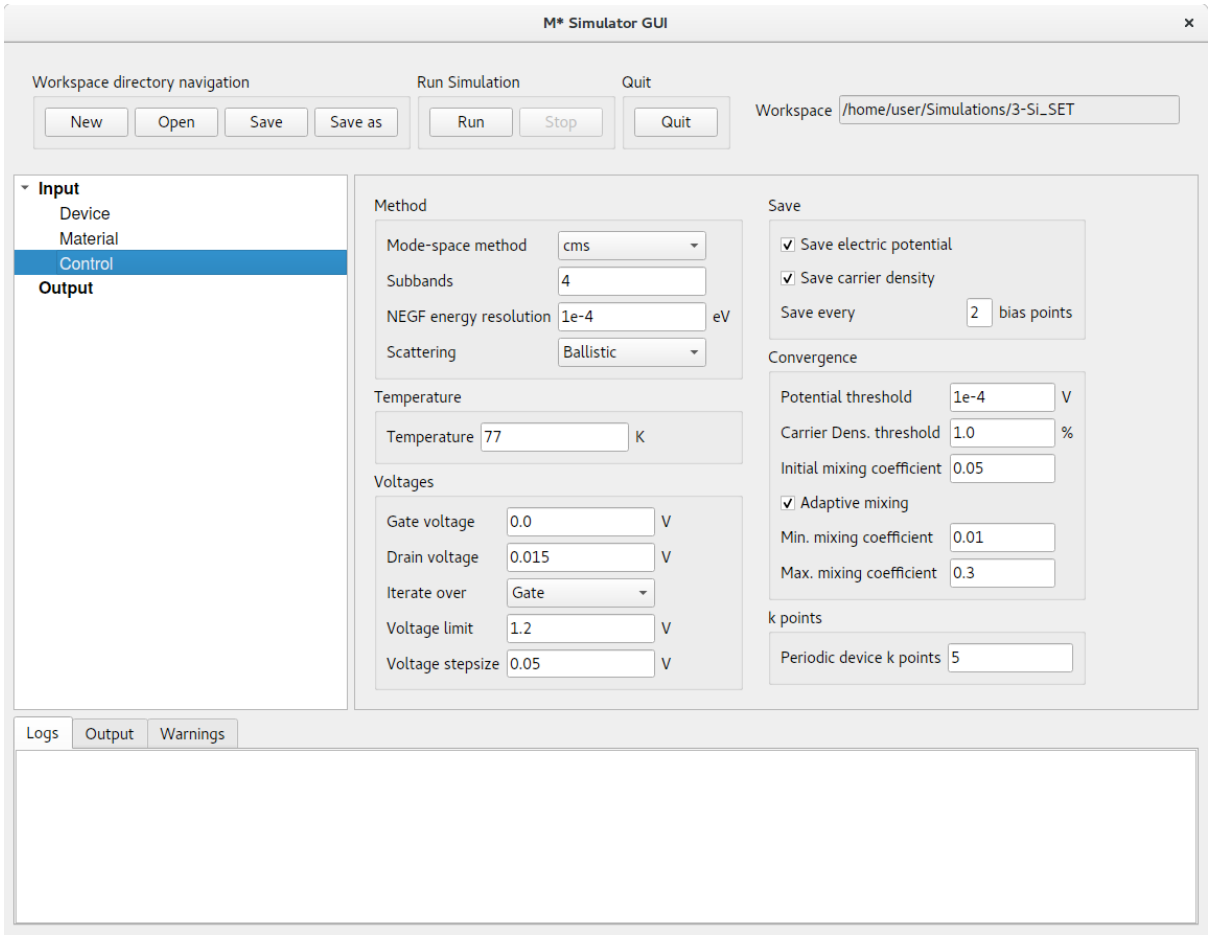


Figure 37: In the `Control` panel, enter parameter values shown in the figure and discussed in the text.

When you have finished setting up all input parameters, click `Run` to begin the simulation. You may follow the simulation's progress tracking the content of the `Logs` tab in the bottom pane. You can inspect your simulation's output as it progresses and bias points are converged; once it's completed, you may plot the device's $I_D - V_{GS}$ characteristics as shown in fig. 38: note the the oscillatory behaviour observed in the linear scale plot (green curve) for $V_{GS} > 0.2$ V.

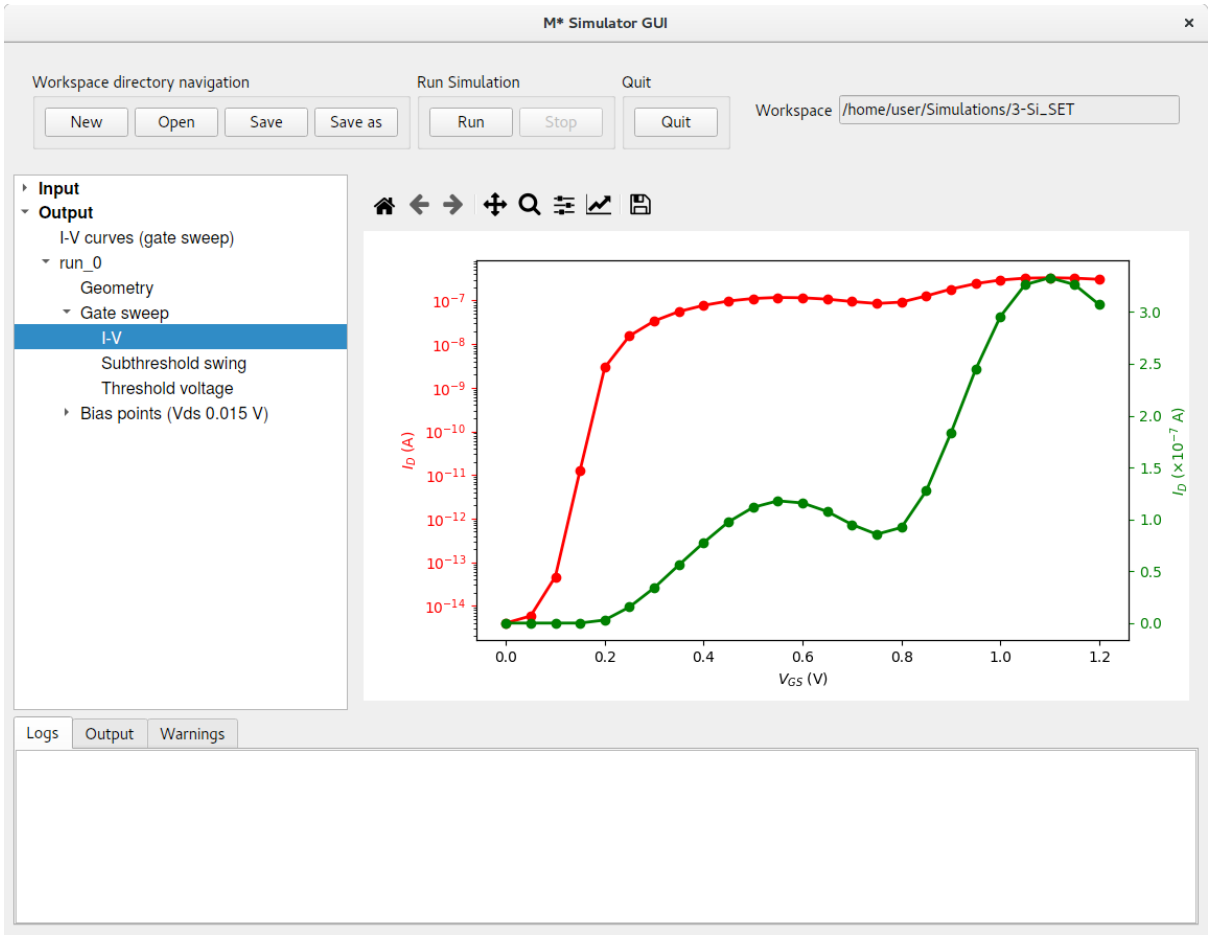


Figure 38: Si single-electron transistor's transfer characteristics at $T = 77$ K.

To begin investigating the properties of this device, let us calculate its threshold voltage by opening the corresponding panel `Output->Threshold Voltage`. You will observe the default algorithm does not correctly compute the threshold voltage as it interprets the device is turning ON around the $[0.8, 1.0]$ V range, as shown in fig. 39. To obtain the correct threshold voltage, we need to manually set the `Fitting boundaries` at the bottom of the plot to indicate the linear regime corresponding to the first drain current increase observed in the plot (green curve). Enter values of 0.3 V and 0.4 V for the `Lower bound` and `Upper bound` fields, respectively, and click `Refresh` to obtain a plot similar to fig. 40.

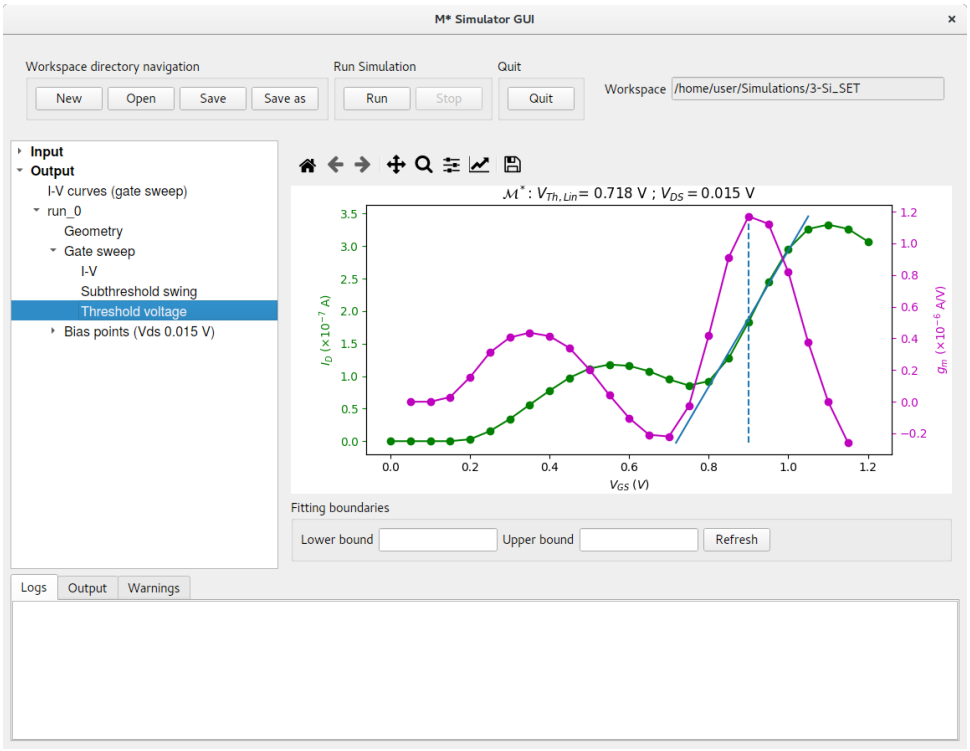


Figure 39: The default $V_{Th}$ extraction algorithm does not detect the correct settings for computing the SET's threshold voltage.

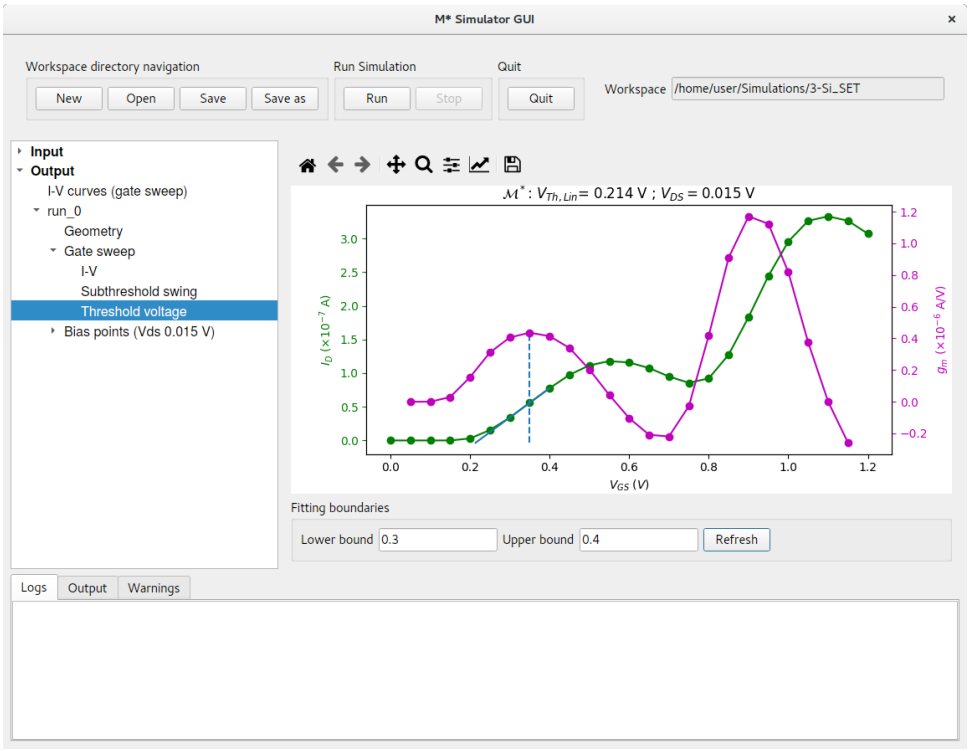


Figure 40: Setting manual fitting range allows computing the correct threshold voltage for this device.

We shall now employ 2D data panels corresponding to a few values of the gate bias to understand the nature of drain current oscillations. Figure 41 shows the local density of states (LDoS), lowest-energy subband for each valley, energy-resolved current, and quasi-Fermi level along the device; as the gate-source bias increases and the first (i.e. lowest-energy) quantised state in the channel begins aligning with occupied states in the source, the device begins to turn ON.

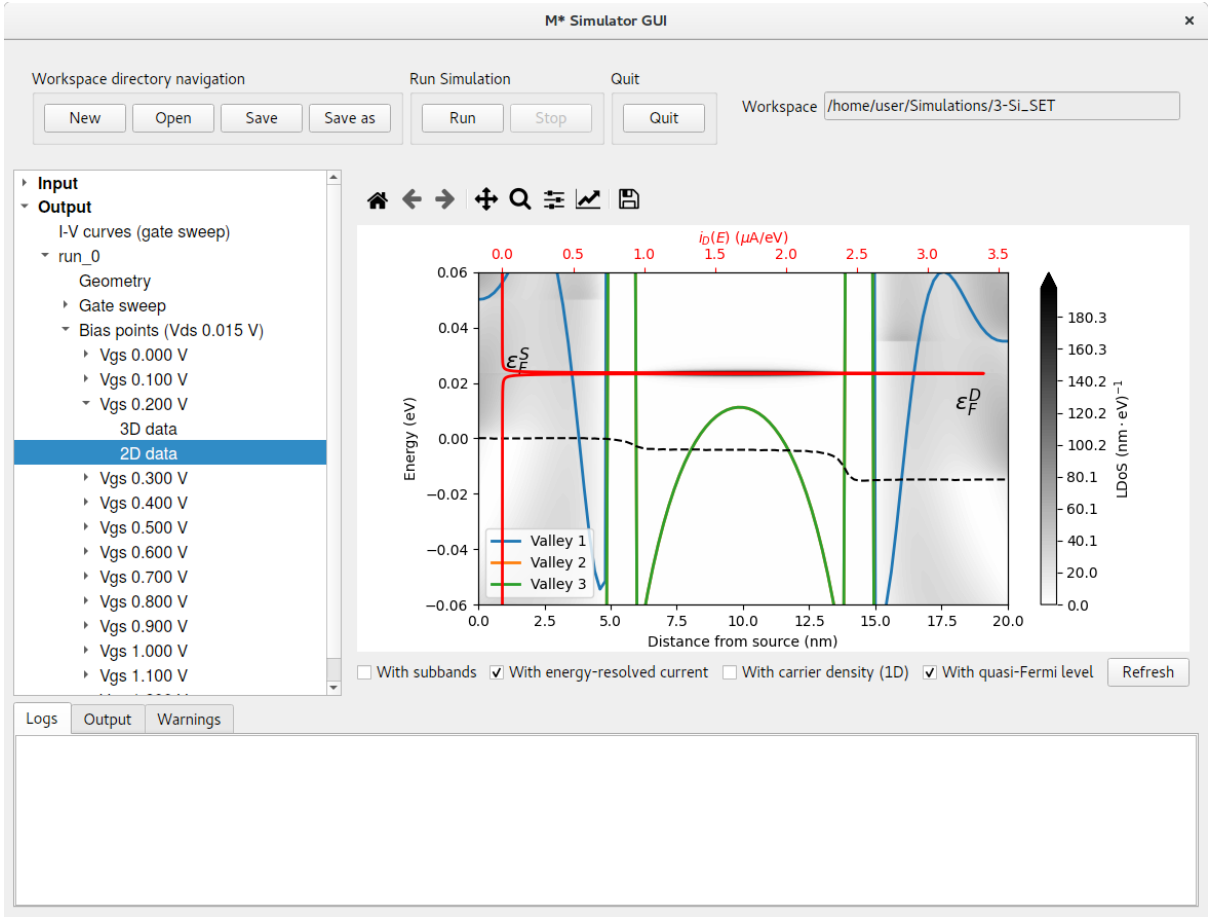


Figure 41: LDoS, energy-resolved current, and quasi-Fermi level for $V_{GS} = 0.2$ V.

Increasing the gate potential continues to shift states in the channel towards lower energies and the we encounter the first maximum in the $I_D - V_{GS}$ characteristics when the lowest-energy quantised state in the channel enters the source-drain bias window (fig. 42).

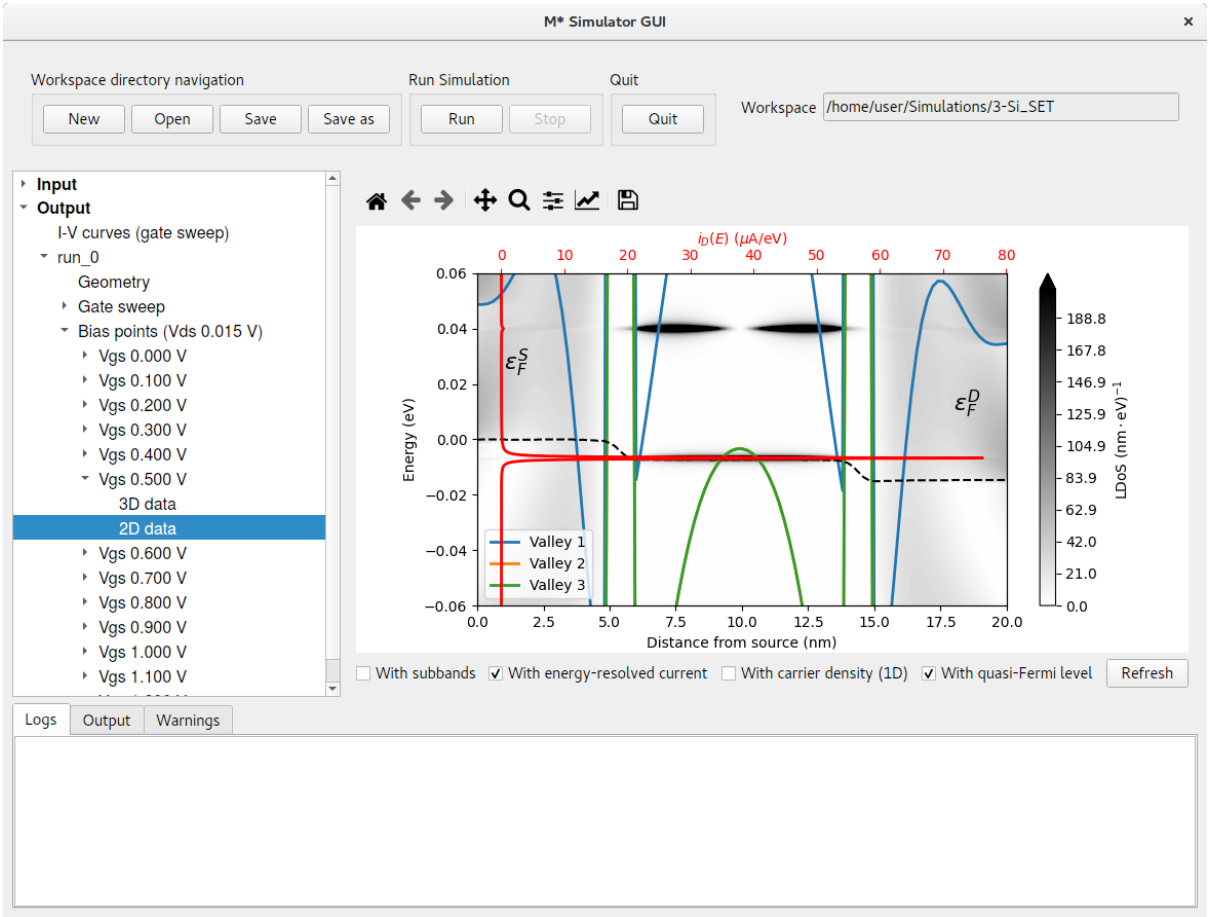


Figure 42: LDoS, energy-resolved current, and quasi-Fermi level for $V_{GS} = 0.5$ V.

For larger gate-source biases, conduction through the second quantised state in the channel begins as it aligns with states occupied in the source, while conduction through the first state in the channel is suppressed due to its alignment with increasingly occupied states in the drain, as depicted in fig. 43; this results in an overall reduction in the drain current observed in the $V_{GS} = [0.6, 0.75]$ V range.

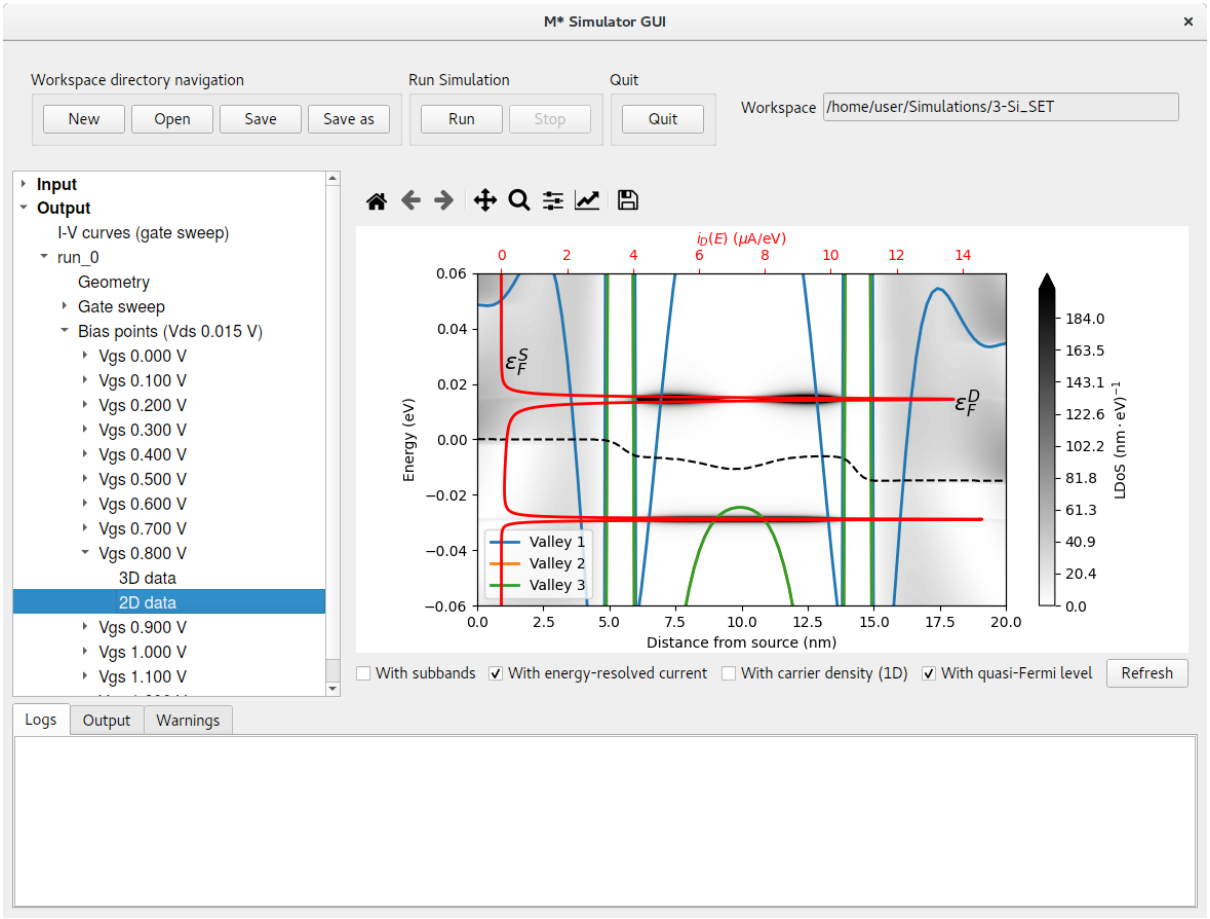


Figure 43: LDoS, energy-resolved current, and quasi-Fermi level for $V_{GS} = 0.8$ V.

Further increases in the gate potential continue to suppress transport through the channel's first quantised state until it becomes irrelevant for electron transport and the second quantised state in the channel dominates instead, as shown in fig. 44.

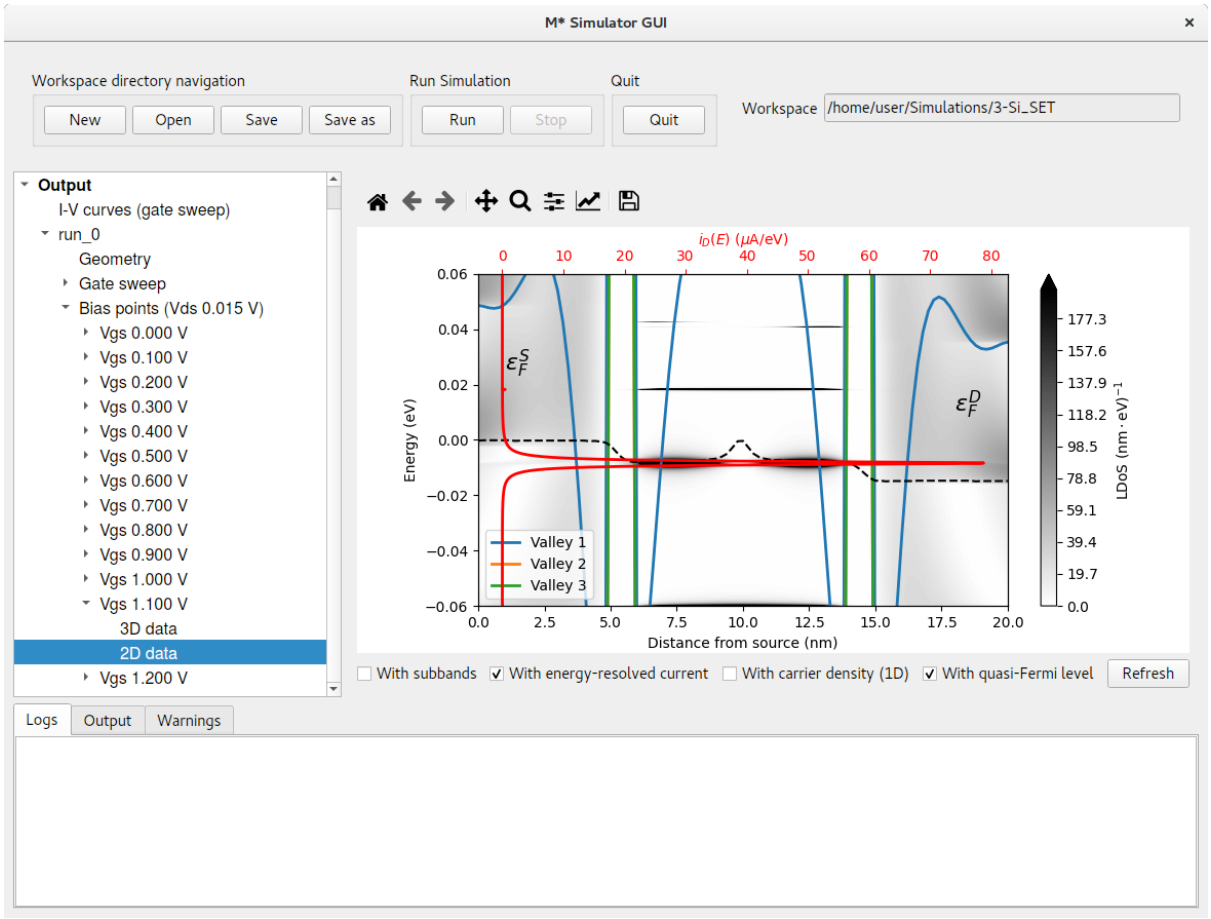


Figure 44: LDoS, energy-resolved current, and quasi-Fermi level for $V_{GS} = 1.1$ V.

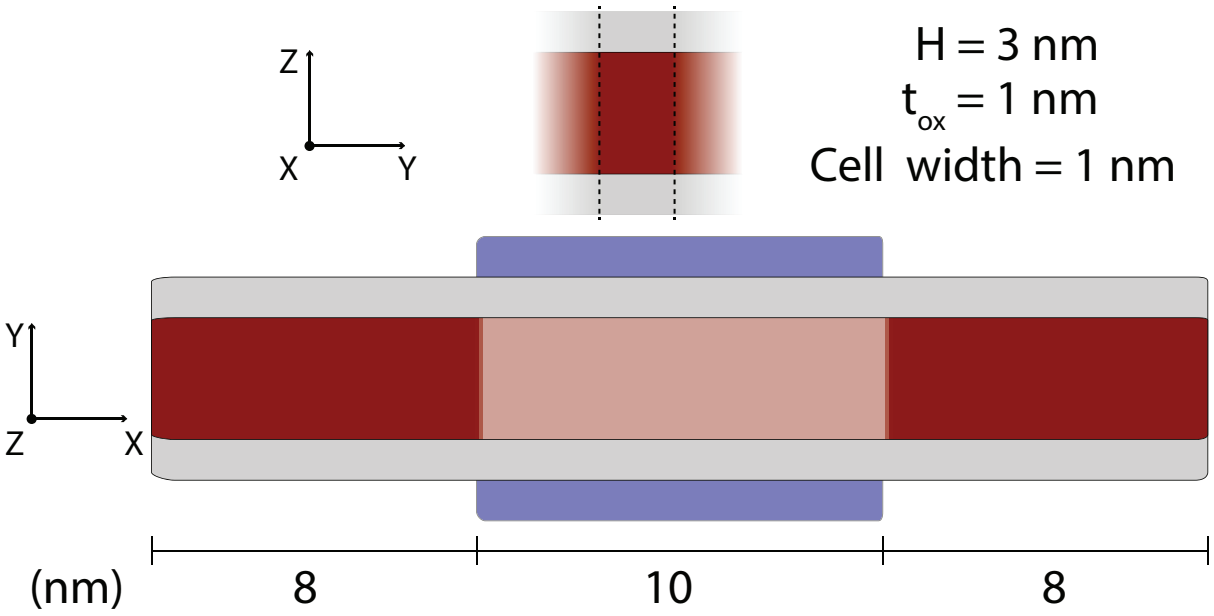


Figure 45: Si double-gate planar FET: Schematic showing the device geometry. Red represents silicon, gray represents silicon dioxide, and blue the gate electrode.

# 4 Tutorial: Silicon p-type planar FET

This tutorial illustrates the usage of two elements not covered in previous test cases:

- **Planar devices** are devices whose width is large enough that we may simulate them as effectively infinitely wide by employing periodic boundary conditions. The top portion of fig. 45 illustrates the device cross-section: we shall simulate a 1 nm-wide cell and employ k-point integration over quantities to compute the properties of an infinitely wide device. The bottom portion of the figure shows the device geometry along the transport direction: a double-gate ultra-thin body (UTB) geometry comprised of a 10 nm long channel and 8 nm long source and drain extensions

- **p-type materials** we note the effective-mass formalism is widely regarded as a crude approximation to the properties of p-type devices due to strong anisotropy, non-parabolicity & bias-dependent tunnelling between heavy hole, light hole, and split-off bands relevant to transport in devices comprised of p-type materials. While $\mathcal{M}^*$ includes parameter sets corresponding to some p-type materials, it is recommended that more sophisticated electronic structure methods are employed when attempting to accurately predict or reproduce the behaviour of real devices

To simulate the properties of this device, open the $\mathcal{M}^*$ GUI and populate input parameters as follows:

- **Device** select `Double-gate planar` as the device type and enter geometrical parameters in accordance with fig. 45 and as shown below in fig. 46. Once you have finished, check the geometry corresponds to the intended design by clicking on the `Preview` tab

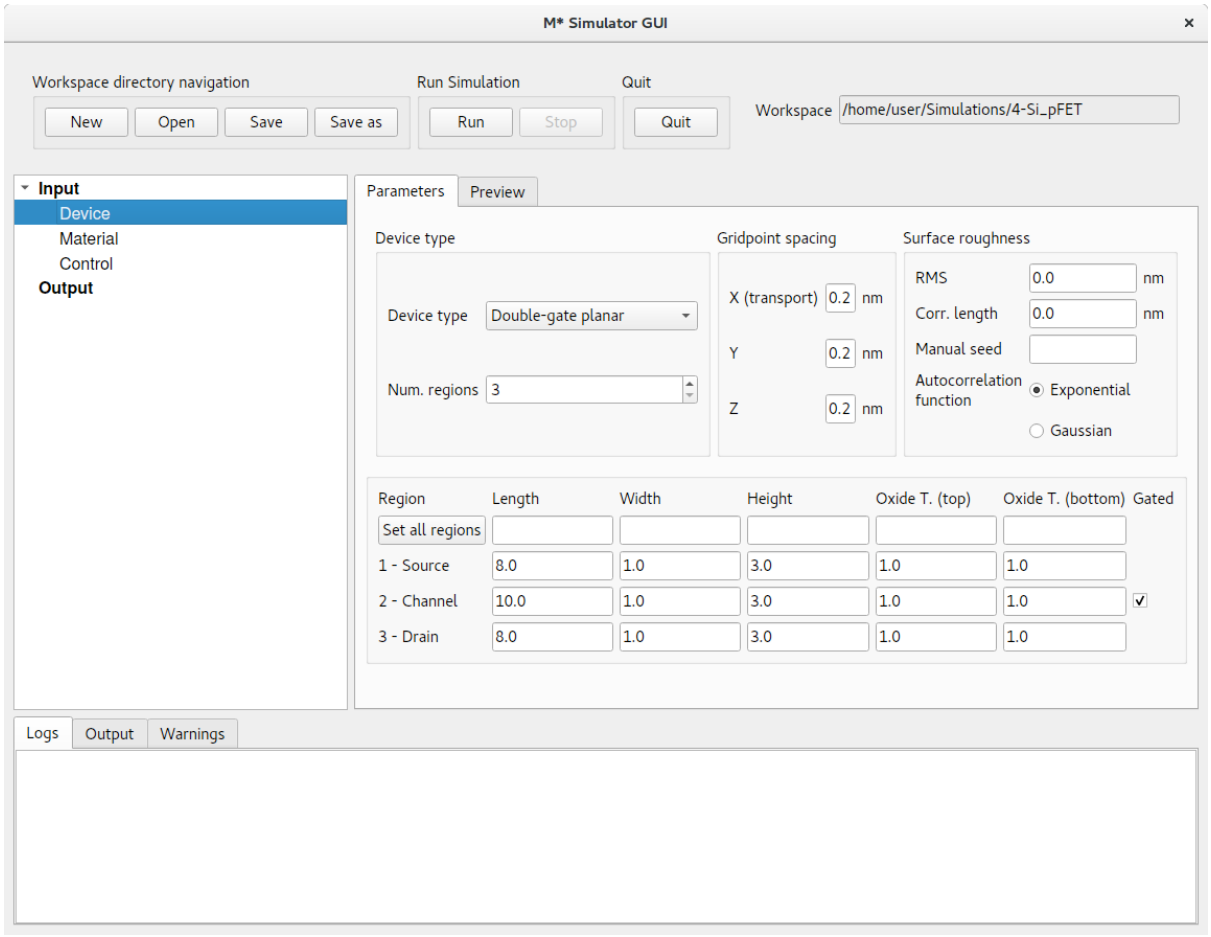


Figure 46: In the `Device` panel, specify a `Double-gate planar` with 3 regions and dimensions shown above.

- **Material** select `Si, p-type` and cycle through regions to set a target carrier concentration of $1 \times 10^{20}$ cm$^{-3}$ in source and drain extensions (i.e. regions 1 & 3), and zero in region 3. Leave the default oxide relative permittivity of $\varepsilon_r = 3.9$ corresponding to $SiO_2$

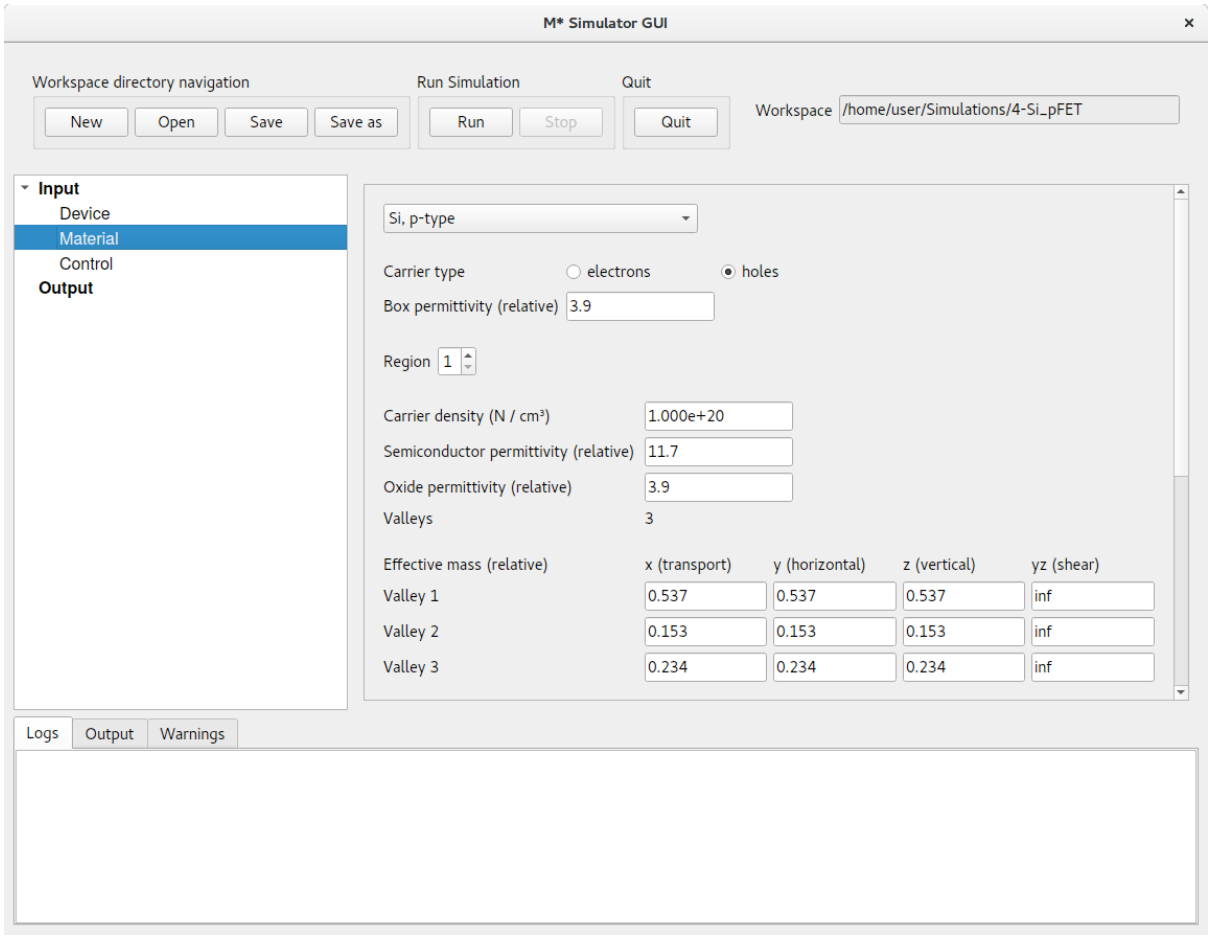


Figure 47: In the `Material` panel, specify a dopant concentration of $1 \times 10^{20}$ cm$^{-3}$ in both source and drain extensions and a value of zero for region 3.

- **Control** select fast uncoupled-mode space (FUMS) as the mode-space method, as is appropriate for devices with such small cross-sectional dimensions, and subbands to 3; note that in devices employing periodic boundary conditions and k-point sampling, this corresponds to using 3 subbands per valley and per k-point. Set a gate voltage sweep covering the $[0.5, -0.4]$ V range in steps of 0.05 V, and a drain voltage of 0.4 V. Enable saving electric potentials and carrier densities and set `Save every [2] bias points` to reduce disk space usage as saving data for every other bias point should provide enough data to study this device. Set the same convergence parameters as in previous tutorials and shown in fig. 48. Finally, we need to enter the amount of k-points along the width direction to incorporate periodicity into our simulation. Set `Periodic device k points` to 7 to perform a first run

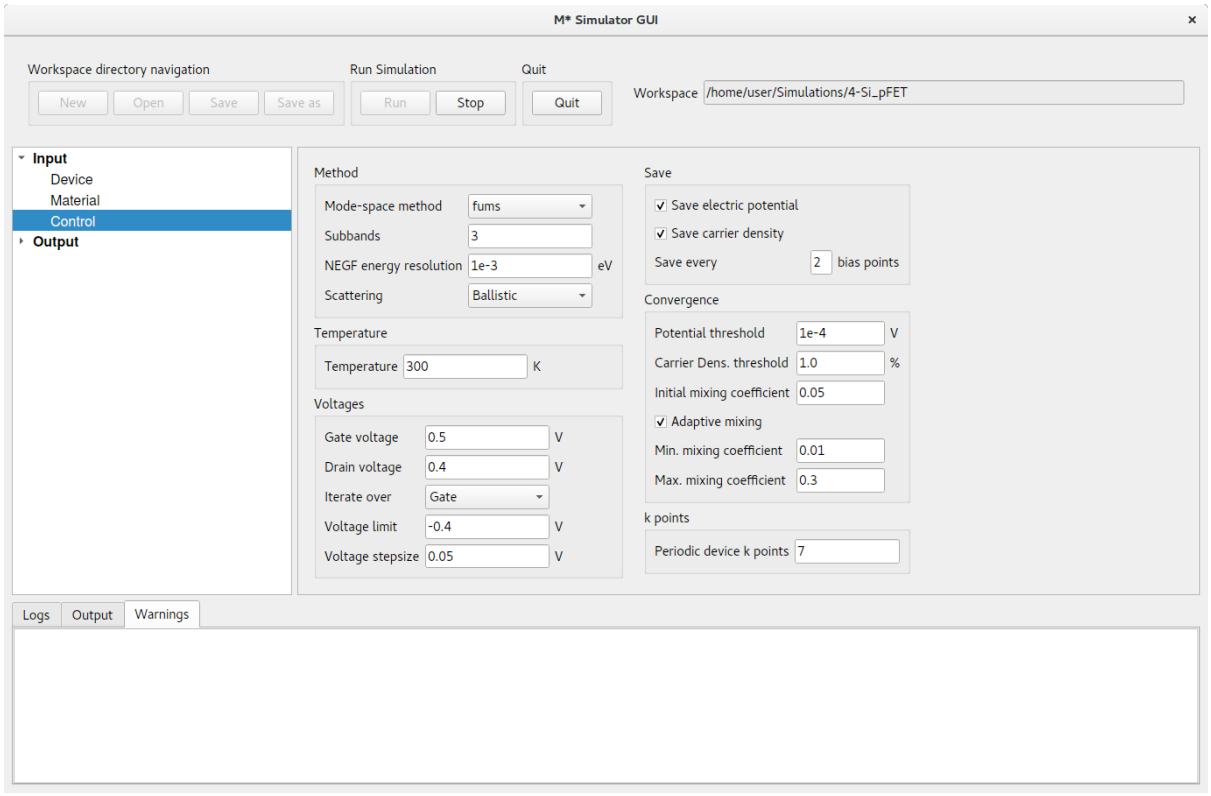


Figure 48: In the `Control` panel, enter parameter values shown in the figure and discussed in the text.

Click `Run` to begin the simulation. Once it has completed, you may visualise output data in the same way as covered in previous tutorials.

## 4.1 k-point sampling

Let us now explore the impact of varying the k-point sampling on the simulated $I_D - V_{GS}$ characteristics of this device. After completing a first simulation performed with `Periodic device k points` set to 7, run two more simulations with a lower (e.g. 5) and a higher (e.g. 9) value, respectively.[3]

Once all simulations have completed, you may compare their transfer characteristics by clicking on `Output->I-V curves (gate sweep)`. Figure 49 shows a comparison between results obtained with 7 k-points and results obtained with 5 k-points; differences can be discerned especially in OFF states where current values vary more than 20%.

[3]Note this input parameter should always be an odd number; if an even number is specified, $\mathcal{M}^*$ will employ the next odd number for the simulation.

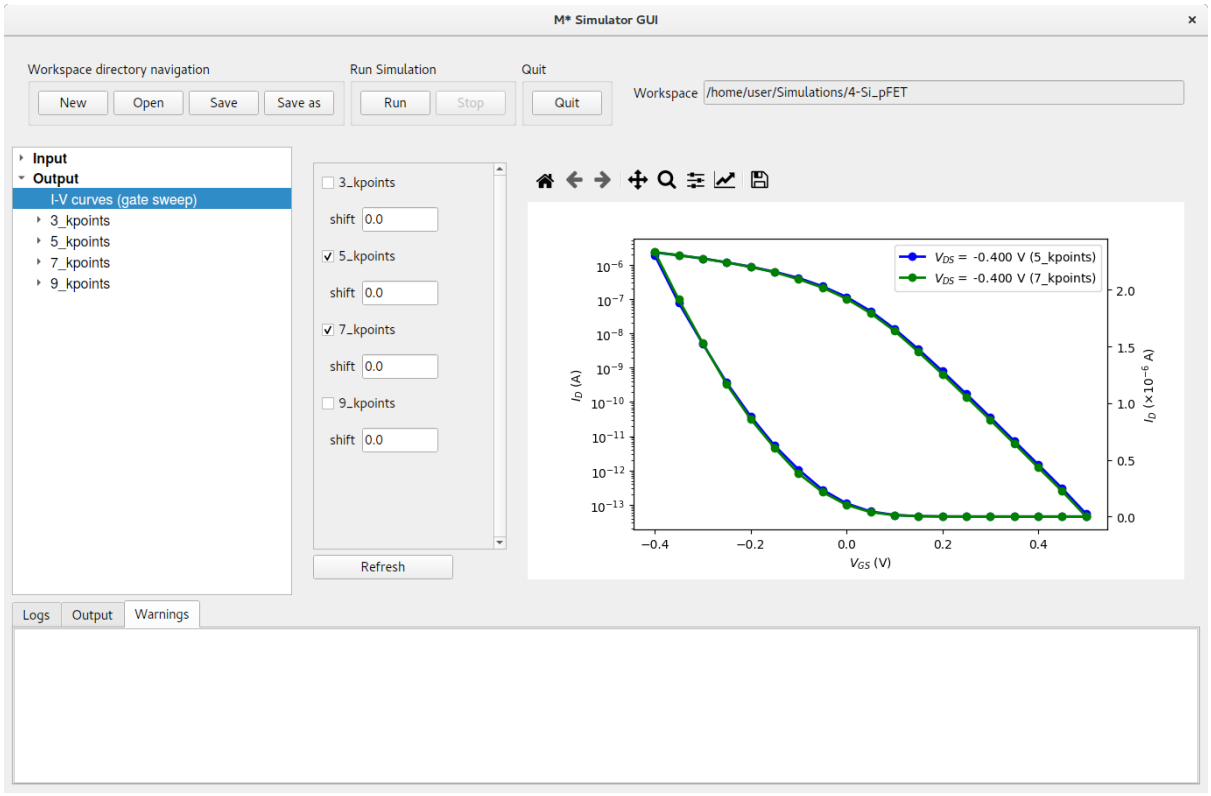


Figure 49: Comparing the reference run (7 k-points) with a 5 k-point run results in noticeable differences, especially for OFF states.

Comparing results obtained with 7 k-points and 9 k-points results in a plot where both curves fully overlap across the entire gate bias range, as shown in fig. 50; the line style and symbol corresponding to the simulation with 9 k-points have been modified for clarity using the toolbar located at the top of the plot. This result indicates the simulation using 7 k-points is appropriately converged. Although wider (narrower) cell widths tend to require a lower (higher) number of k-points to reach convergence, other system properties may affect appropriate values for each system. It is highly recommended convergence with respect to this parameter is checked for each device.

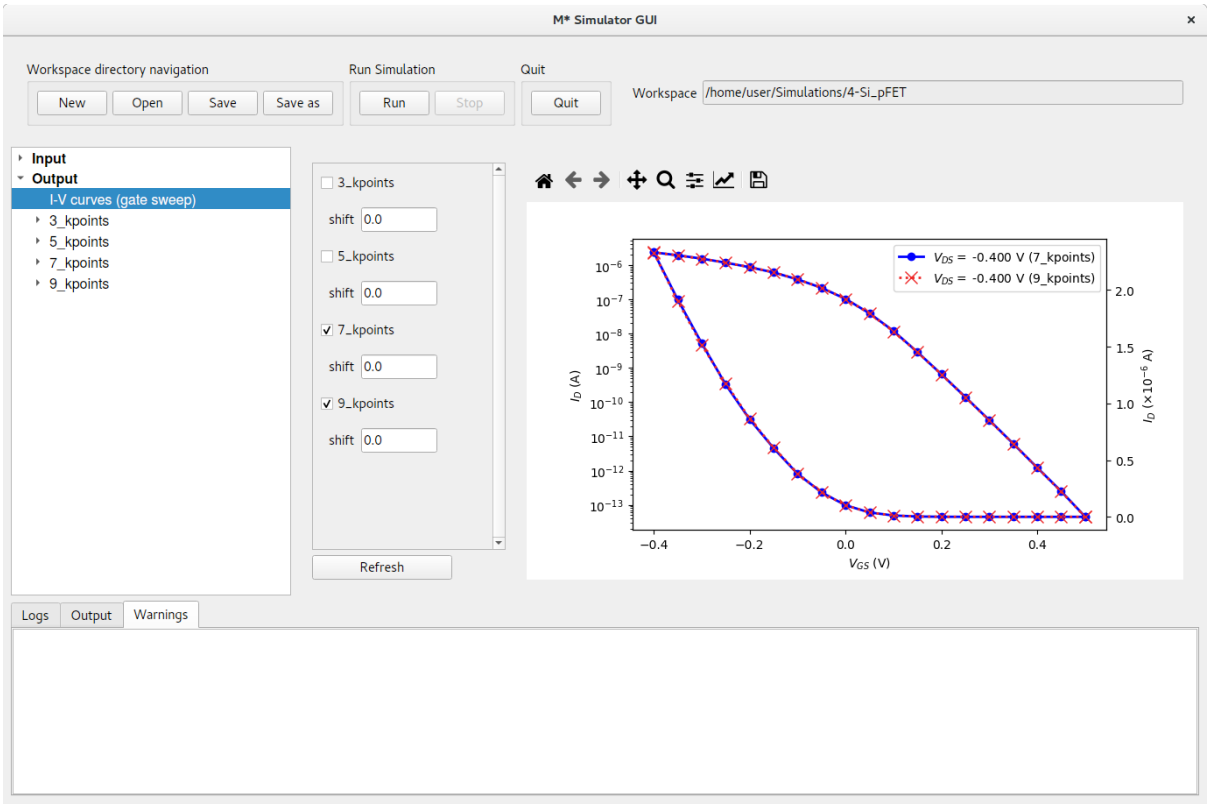


Figure 50: Comparing the reference run (7 k-points) with a 9 k-point run results in curves that fully overlap across the entire gate bias range.

Finally, fig. 51 shows a comparison between curves computed with 7 k-points, and 3 k-points. In this case differences between both curves is evident in both OFF states and ON states. Note differences in OFF states tend to be larger than in ON states, as can be observed from the semilogarithmic plot.

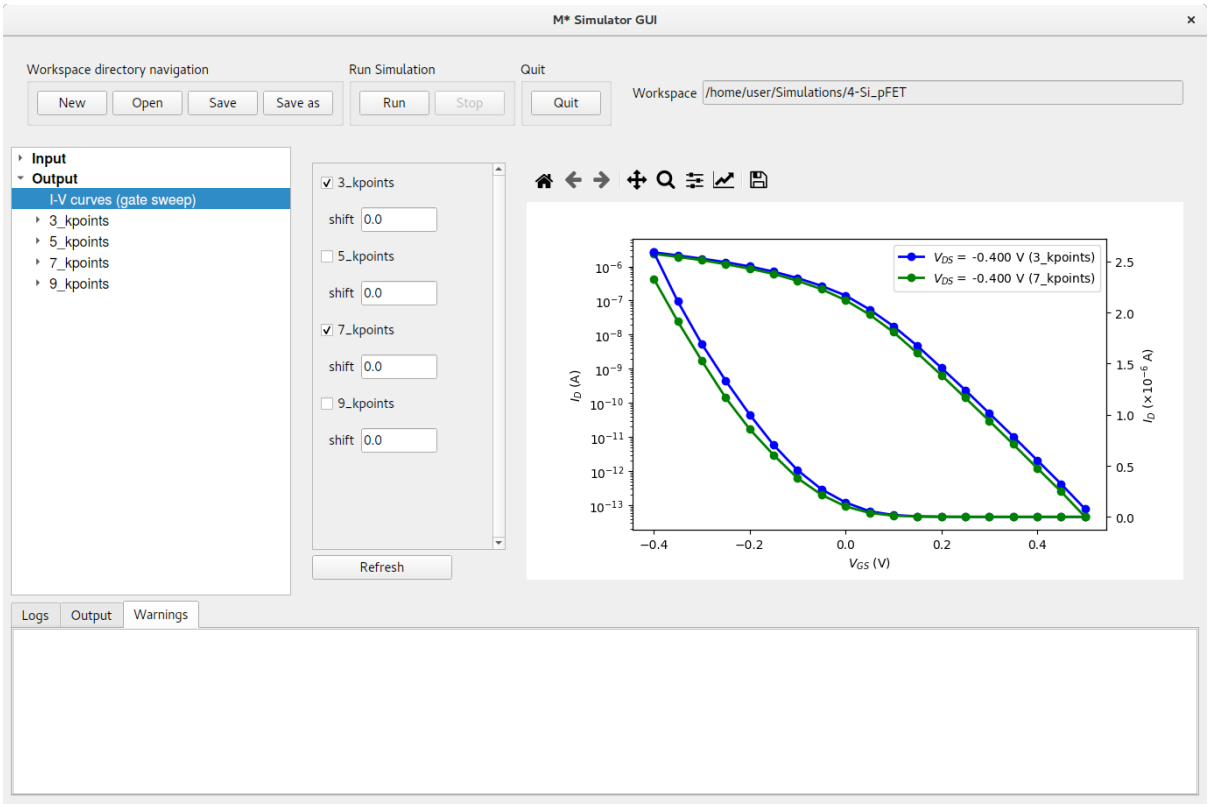


Figure 51: Comparing the reference run (7 k-points) with a 3 k-point run results in noticeable differences in both ON and OFF states.

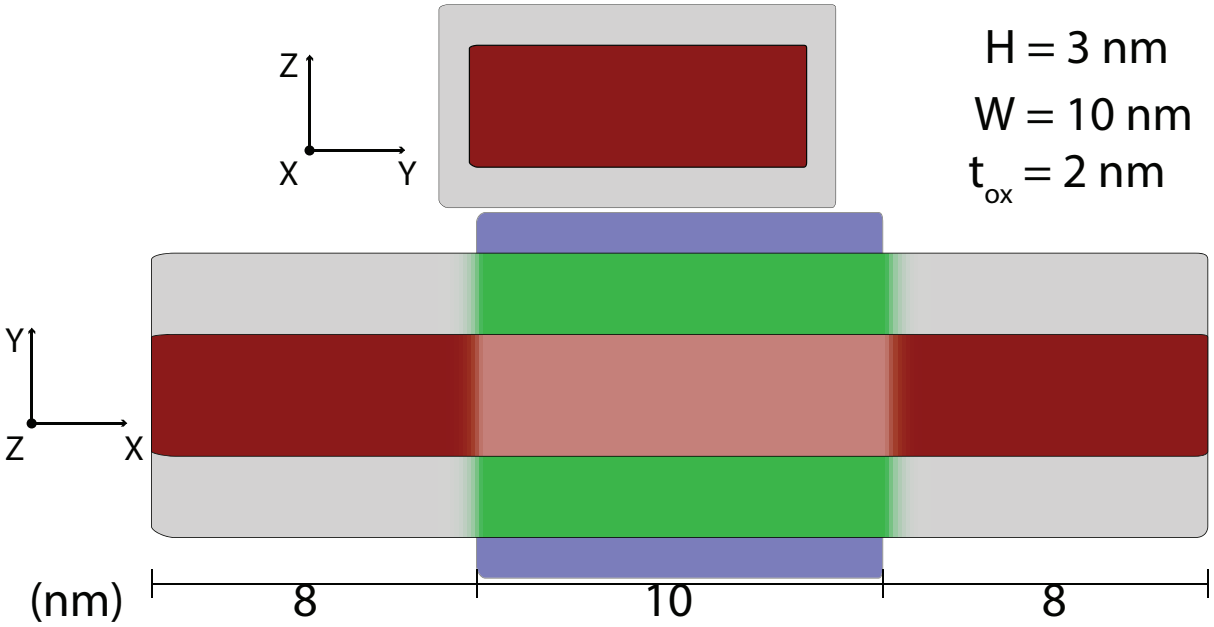


Figure 52: $In_{0.53}Ga_{0.47}As$ nanosheet FET: Schematic showing the device geometry. Red represents $In_{0.53}Ga_{0.47}As$, gray represents a low-$\kappa$ oxide, green a high-$\kappa$ oxide, and blue the gate electrode.

# 5 Tutorial: $In_{0.53}Ga_{0.47}As$ nanosheet FET

In this tutorial we simulate a nanosheet-based device comprised of a III-V channel material. Nanosheet device types allow simulating the properties of quasi-planar devices where effects due to the semiconductor's finite width are explicitly treated. To set up this simulation start a new $\mathcal{M}^*$ workspace and set input parameters as:

- **Device** select `Double-gate nanosheet` as the device type and enter geometrical parameters in accordance with fig. 52 and as shown below in fig. 53. Once you have finished, check the geometry corresponds to the intended design by visualising it in the `Preview` tab

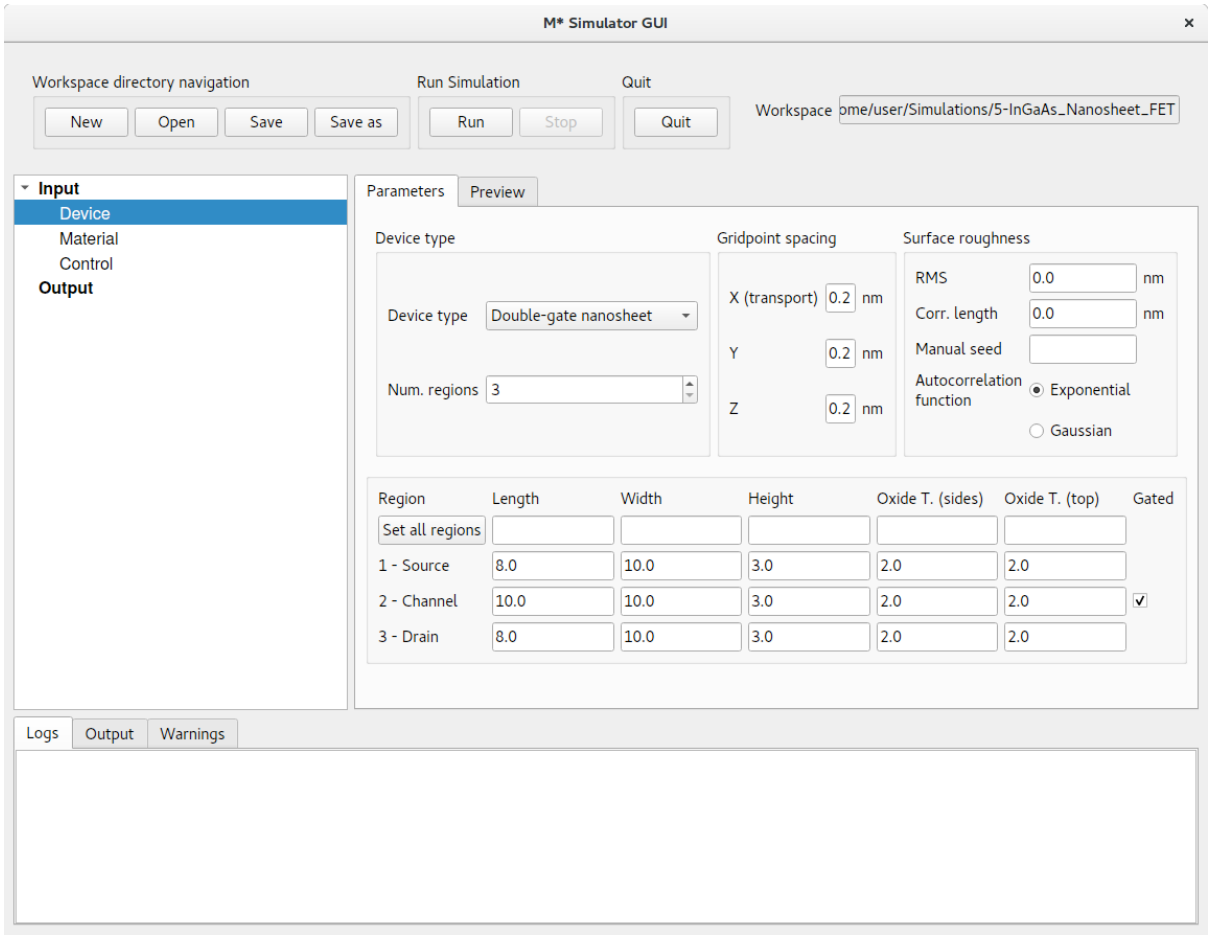


Figure 53: In the `Device` panel, specify a `Double-gate nanosheet` with 3 regions and dimensions shown above.

- **Material** select `In(0.53)Ga(0.47)As, (010)/<100>, n-type` and cycle through regions to set a target carrier concentration of $5 \times 10^{19}$ cm$^{-3}$ in source and drain extensions (i.e. regions 1 & 3), and zero in region 3. Input an oxide relative permittivity of $\varepsilon_r = 4.0$ (low-$\kappa$ oxide) in source and drain extensions, and a value $\varepsilon_r = 20.0$ (high-$\kappa$ oxide) in the channel. The low-$\kappa$ oxide will reduce capacitive coupling between the gate electrode and source/drain extension regions

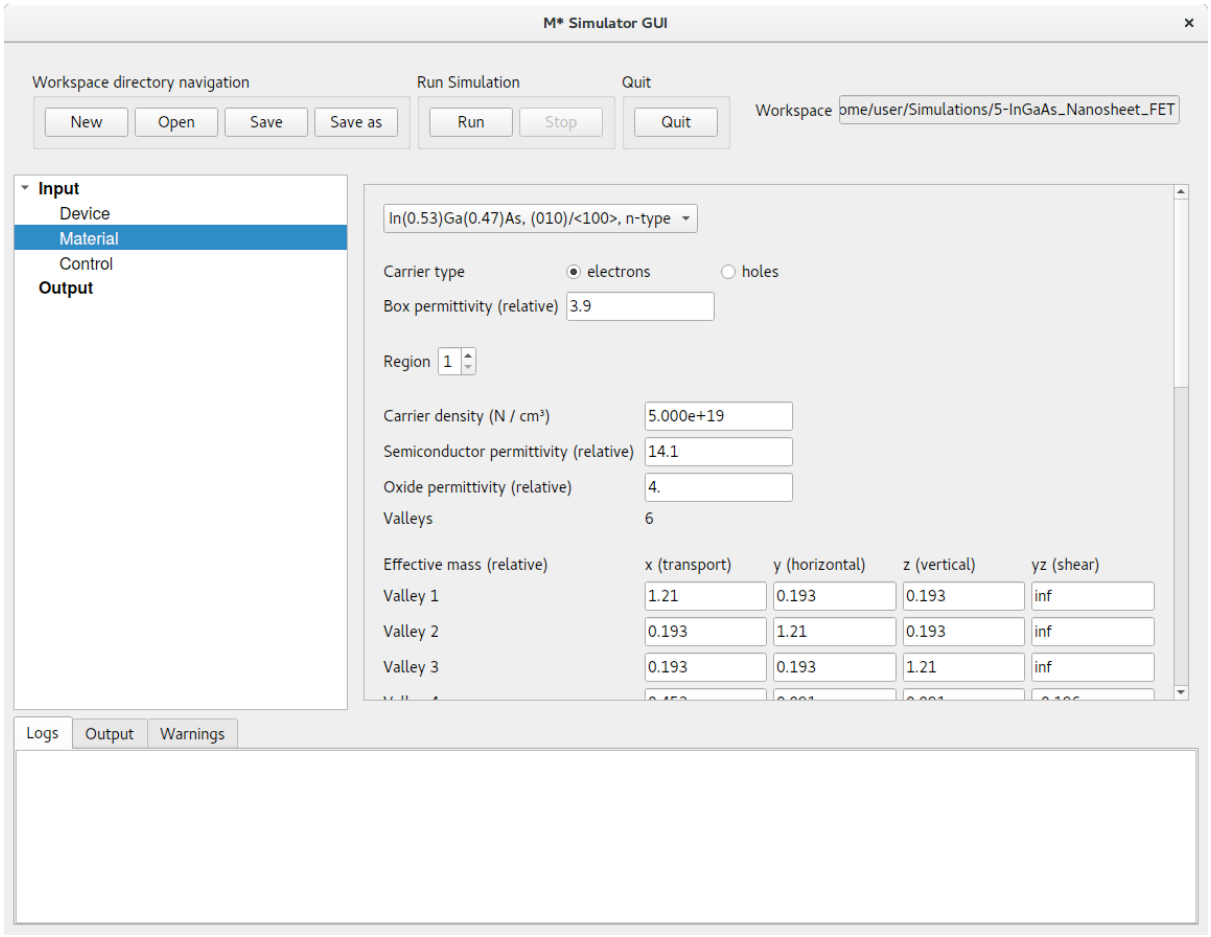


Figure 54: In the `Material` panel, specify a carrier concentration of $5 \times 10^{19}$ cm$^{-3}$ and an oxide relative permittivity $\varepsilon_r = 4.0$ in both source and drain extensions, and a zero carrier concentration and $\varepsilon_r = 20.0$ in the channel.

- **Control** select fast uncoupled-mode space (FUMS) as the mode-space method, and subbands to 6. Set a gate voltage sweep covering the $[0.0, 0.85]$ V range in steps of 0.05 V, and a drain voltage of 0.05 V. Enable saving electric potentials and carrier densities and set `Save every [2] bias points` to reduce disk space usage. Set the same convergence parameters as in previous tutorials and shown in fig. 55

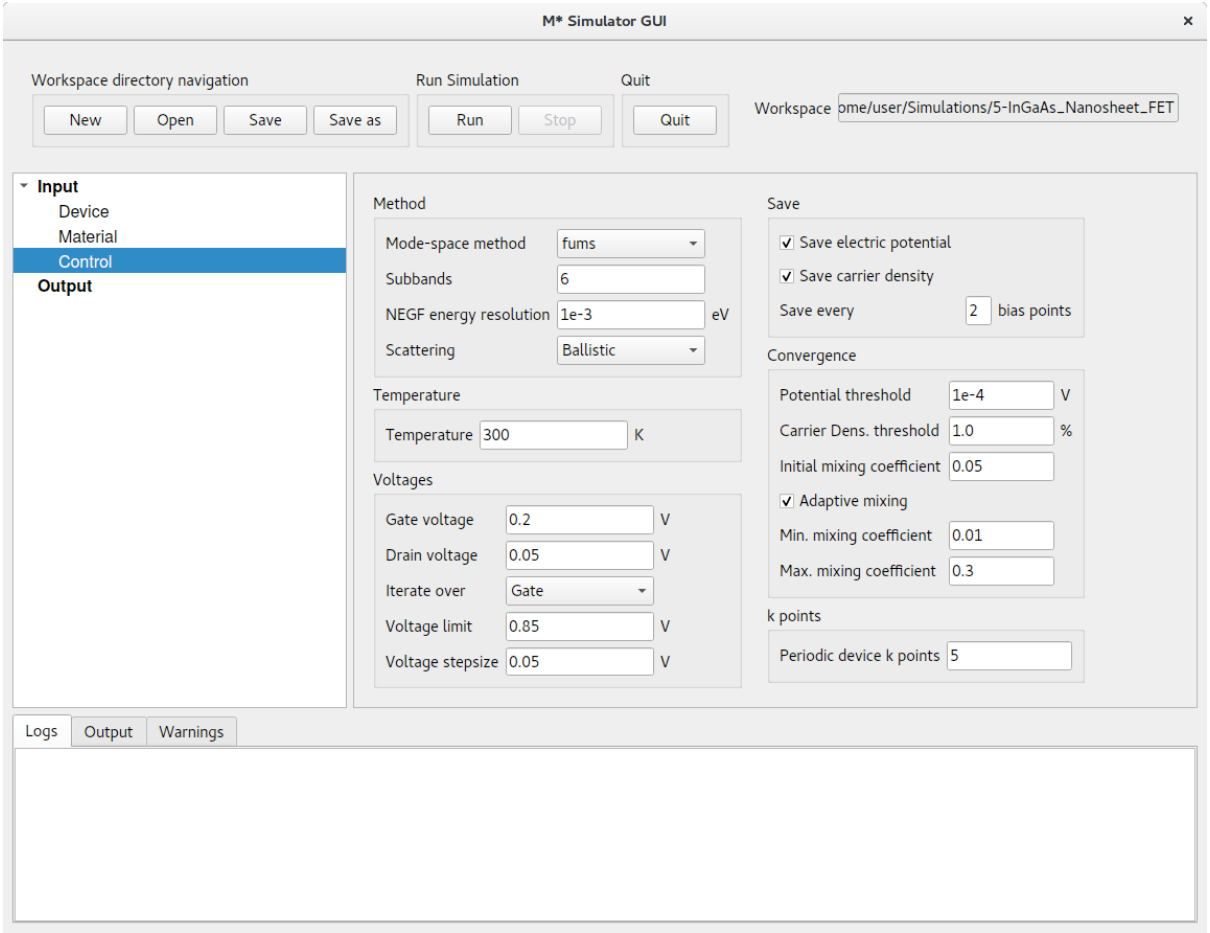


Figure 55: In the `Control` panel, enter parameter values shown in the figure and discussed in the text.

Click `Run` to begin the simulation. Once completed, you may visualise the 3D quantities to observe the influence of the device's finite width on both electric potential and carrier density, as shown in figs. 56 and 57 for an ON state.

Next, inspect `2D data` for various bias point to visualise plots similar to figs. 58 and 59 (OFF and ON states, respectively). We can observe that the properties of this device are dominated by valleys 1 - 3, corresponding to the three X valleys in $In_{0.53}Ga_{0.47}As$. The significantly lower effective masses of valleys 4 & 5 (L valleys), and valley 6 ($\Gamma$ valley) along cross-sectional dimensions result in larger confinement-induced shifts to their associated subbands towards higher energies, rendering their impact on the properties of this device negligible.

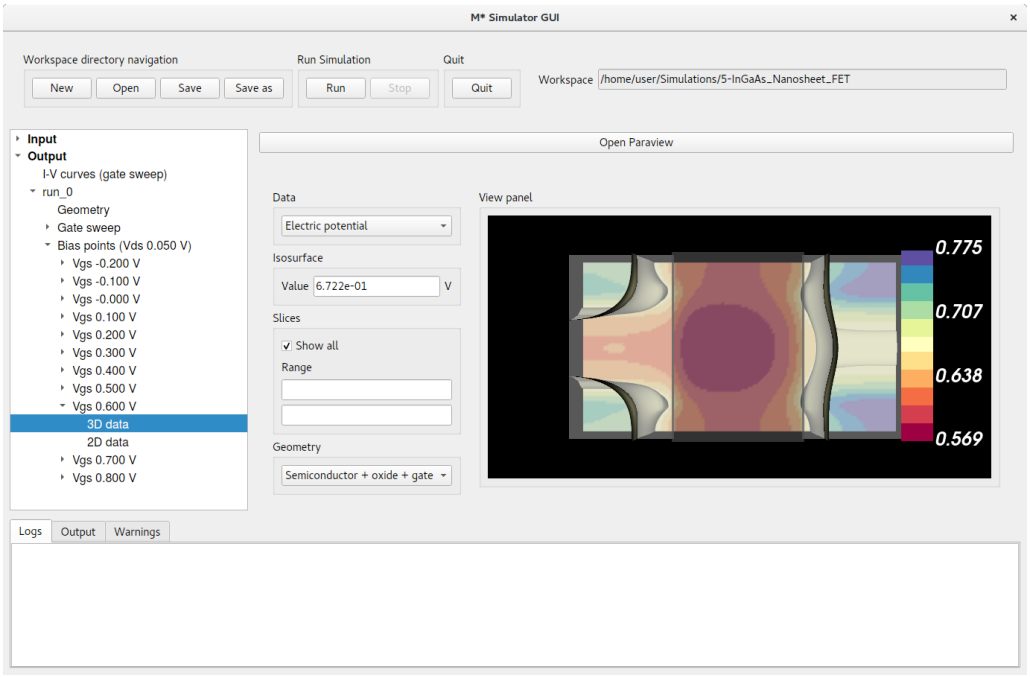


Figure 56: Electric potential at $V_{GS} = 0.6$ V (ON state).

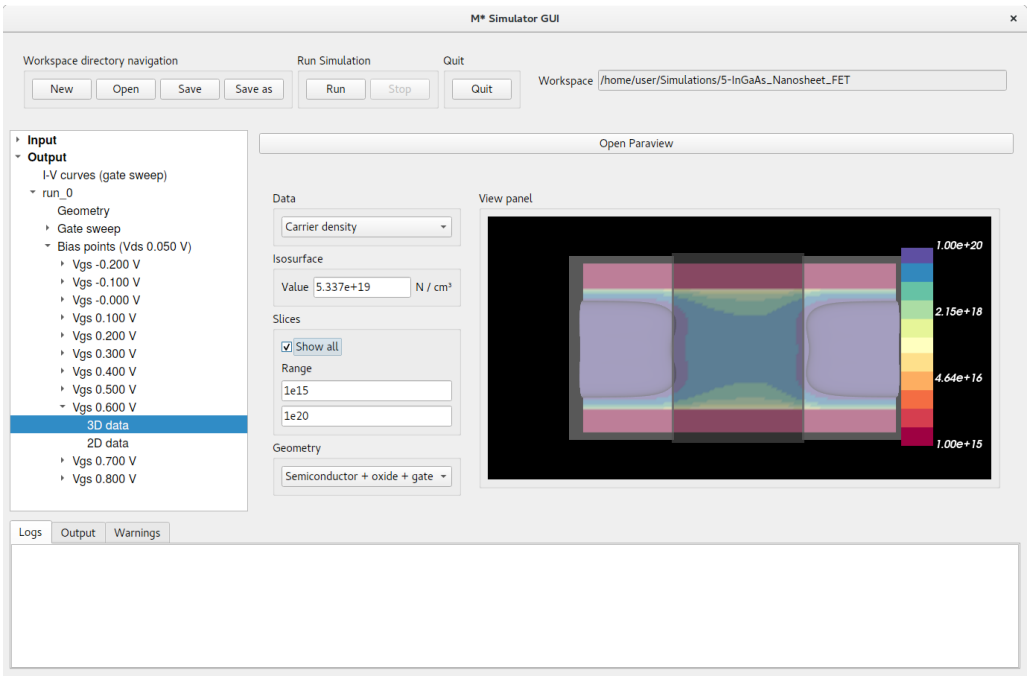


Figure 57: Carrier density at $V_{GS} = 0.6$ V (ON state). Note the range for the contour plot has been manually set to $[10^{15}, 10^{20}]$ cm$^{-3}$

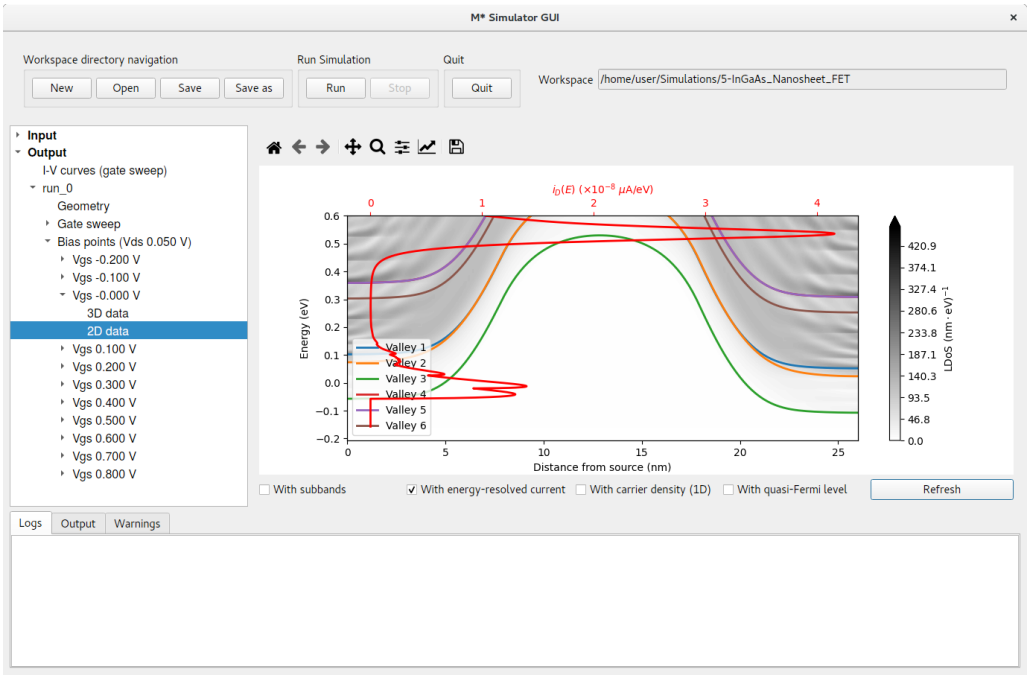


Figure 58: Local density of states, lowest subband for each valley, and energy-resolved current at $V_{GS} = 0.0$ V (OFF state).

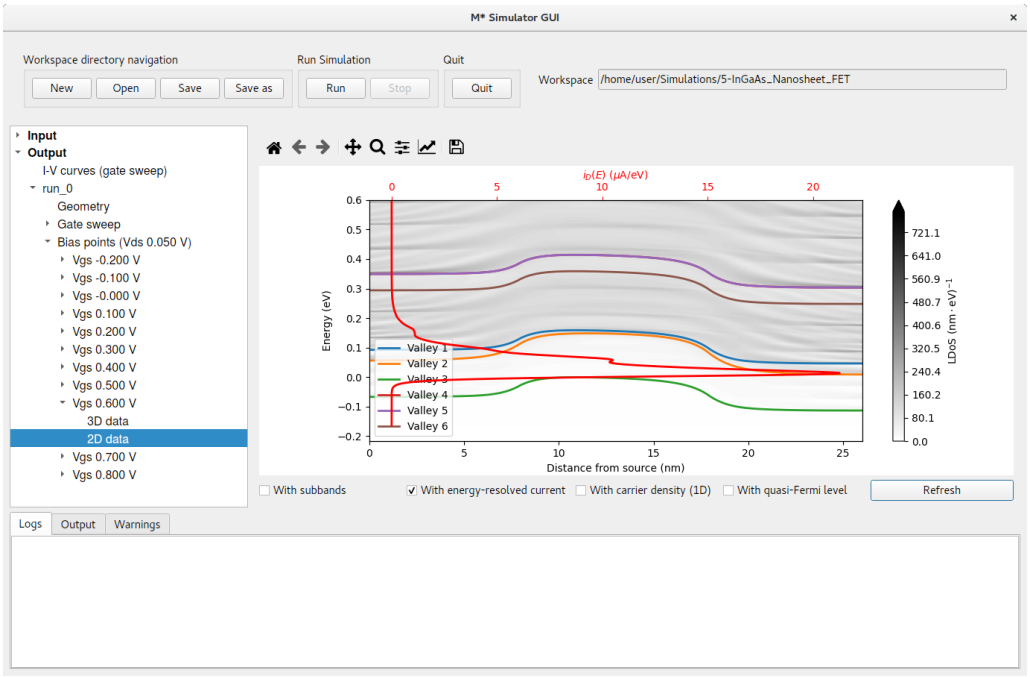


Figure 59: Local density of states, lowest subband for each valley, and energy-resolved current at $V_{GS} = 0.6$ V (ON state).

To explore the geometrical dependence of confinement-induced energy shifts and their impact on device operation, let us simulate a similar device with a thicker channel:

- **Device** edit the device geometry by modifying the value of `Height` fields with a value of 6 nm for all three regions
- **Control** edit the gate voltage sweep range to $[-0.2, 0.85]$ V to cover more OFF states

Click `Run` to begin the simulation. Once finished, let us make identifying both devices easier by renaming `run_0` to `H=3nm`, and `run_1` to `H=6nm`. We begin our analysis by visualising the corresponding I-V characteristics, shown in fig. 60. Note the device appears to turn ON in two stages with a first contribution appearing for $V_{GS} > 0.2$ V, and a second contribution for $V_{GS} > 0.6$ V.

Plotting 2D data for $V_{GS} = 0.2$ V illustrates device operation around the point where the first contribution begins. Figure 61 shows the device begins turning ON when the bottom subband in valley 6 ($\Gamma$ valley) comes in alignment with the source's Fermi level. Note that valley 6 is lower in energy in this device and the first subband in all six valleys lie at energies below 0.2 eV above the source Fermi level, making them all relevant to this device's properties. The reduced confinement in this structure with larger cross-sectional dimensions has dramatically changed the electronic structure compared to the device based on a nanosheet with 3 nm height.

Figure 62 shows the 2D data panel for $V_{GS} = 0.6$ V. The energy-resolved current reveals that the second contribution observed in the I-V characteristics occurs for gate bias values high enough such that valleys 1 - 3 (i.e. X valleys) in the channel are aligned with the Fermi level at the source.

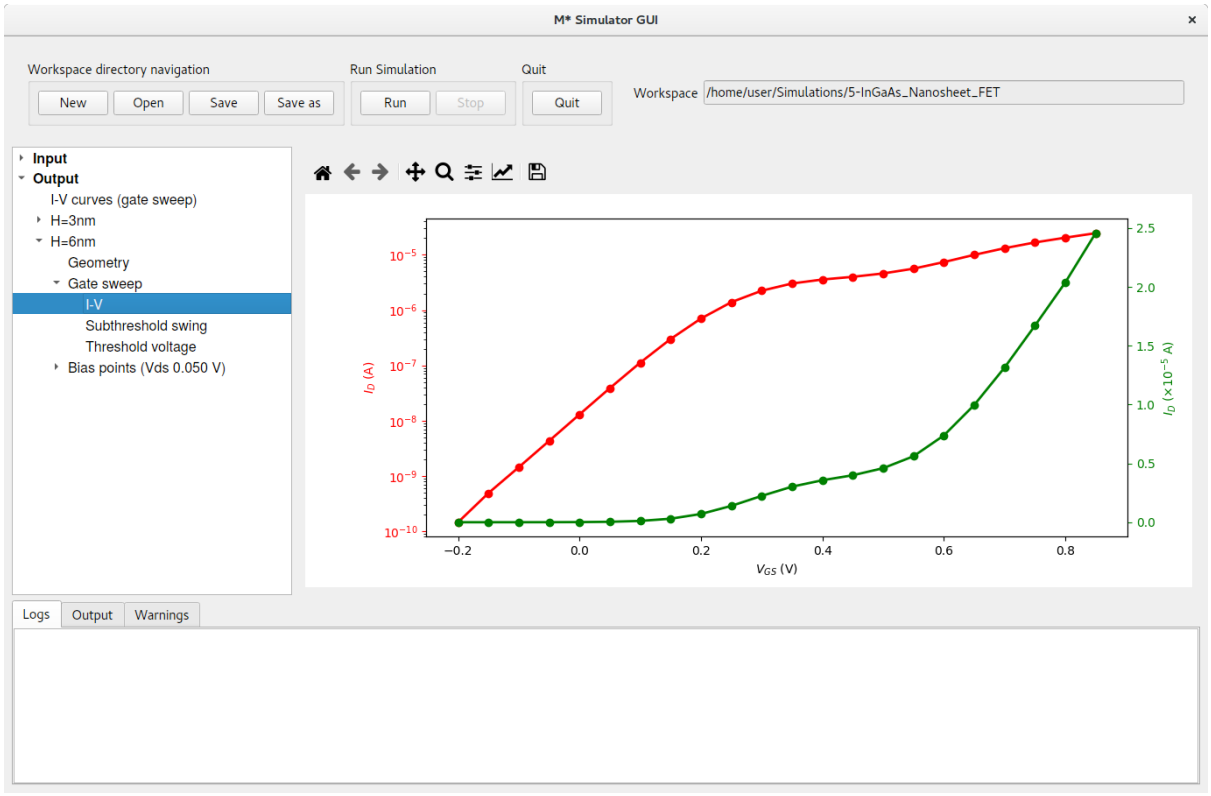


Figure 60: $I_D - V_{GS}$ characteristics for device with 6 nm height.

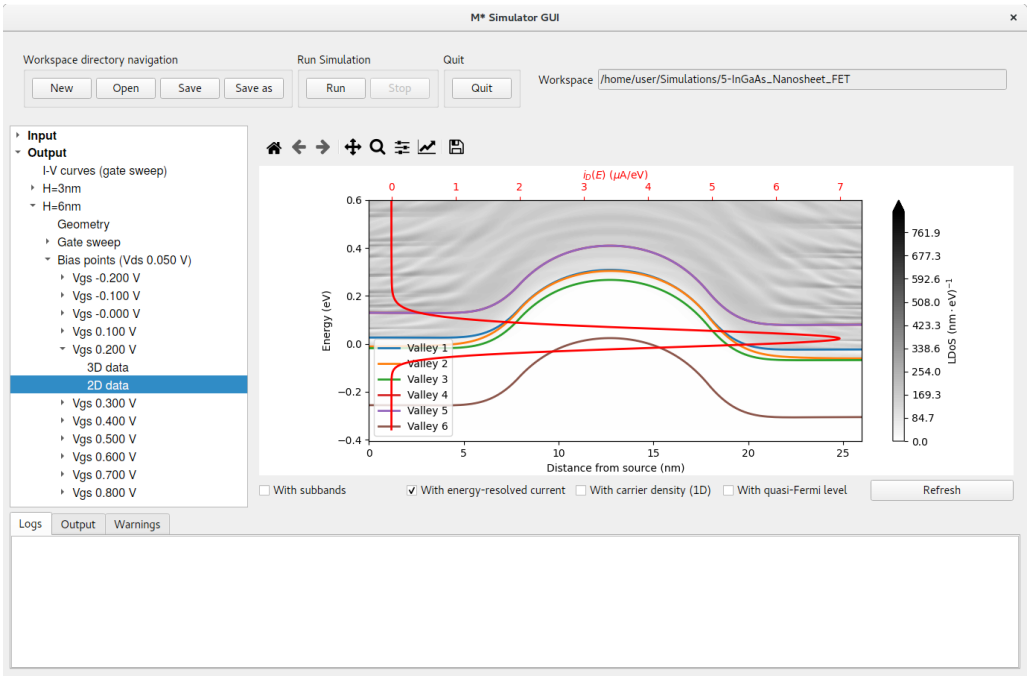


Figure 61: Local density of states, lowest subband for each valley, and energy-resolved current for the thicker device at $V_{GS} = 0.2$ V (ON state).

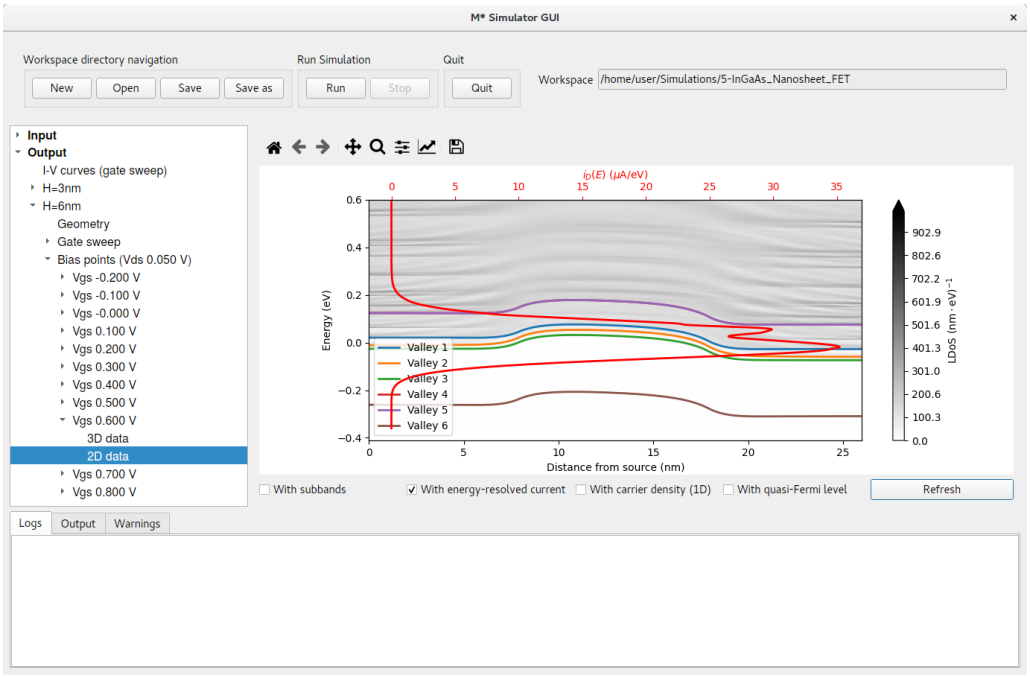


Figure 62: Local density of states, lowest subband for each valley, and energy-resolved current for the thicker device at $V_{GS} = 0.6$ V (ON state).

In order to compare both devices' in a more meaningful manner, let us shift their I-V characteristics by their respective threshold voltages. Extracting the threshold voltage of the device with H= 3 nm should be straightforward, resulting in a value of $V_{Th,Lin} = 0.555$ V (fig. 63). Attempting to obtain a threshold voltage value for the thicker device requires some tweaking: by default, $\mathcal{M}^*$ attempts a fit around the point of maximum conductance ($g_m$, right axis in fig. 64). Manually enter lower and upper bounds of $[0.25, 0.35]$ V and click `Refresh` to recalculate a fit around the first conductivity maximum to obtain a more appropriate value of $V_{Th,Lin} = 0.138$ V, as shown in fig. 64. Finally, click on `Output->I-V curves ( gate sweep)` and enter `shift` values corresponding to each device's $-V_{Th,Lin}$ (with opposite sign) to align their threshold voltage with $V_G = 0$ V. Click `Refresh` to generate a plot similar to fig. 65.

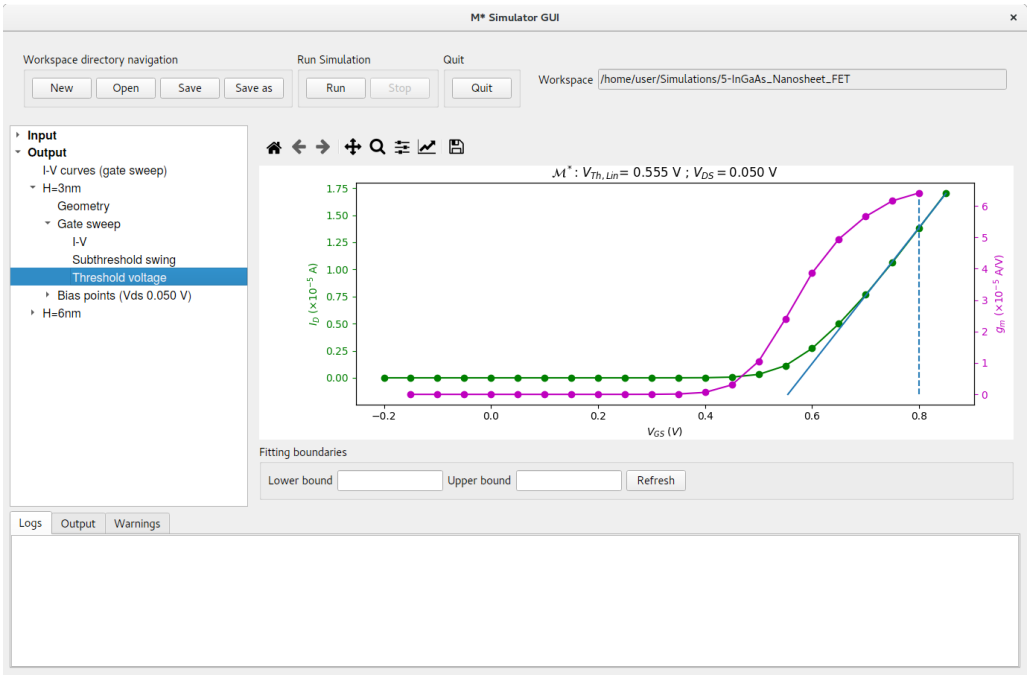


Figure 63: Threshold voltage extraction for the device based on a nanosheet with a height of 3 nm.

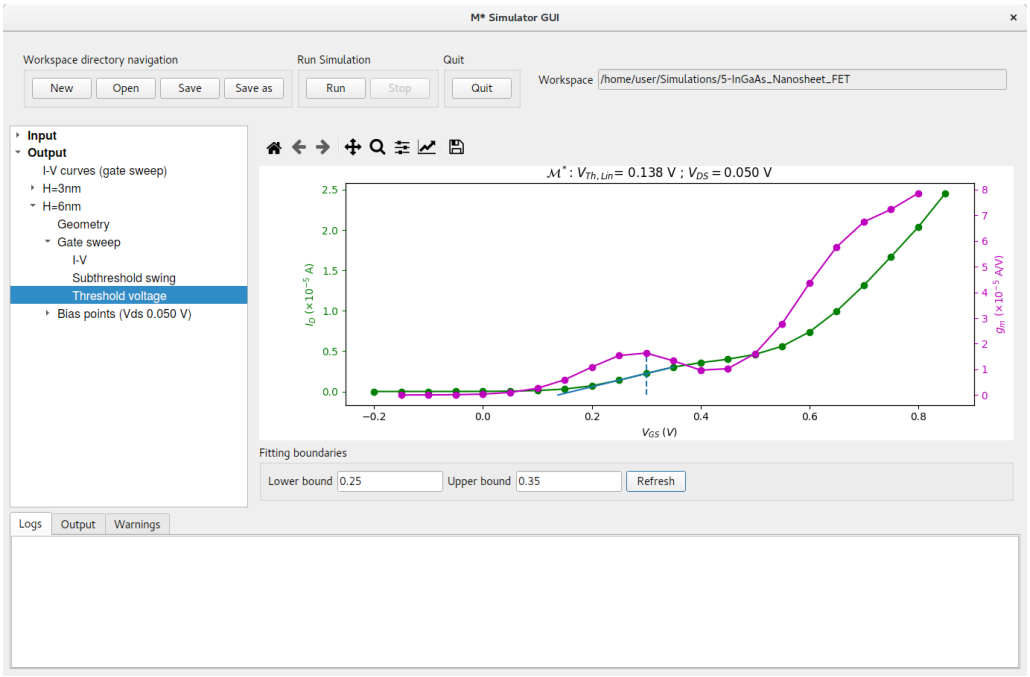


Figure 64: Threshold voltage extraction for the device based on a nanosheet with a height of 6 nm. Note that a manual range has been specified for the fit.

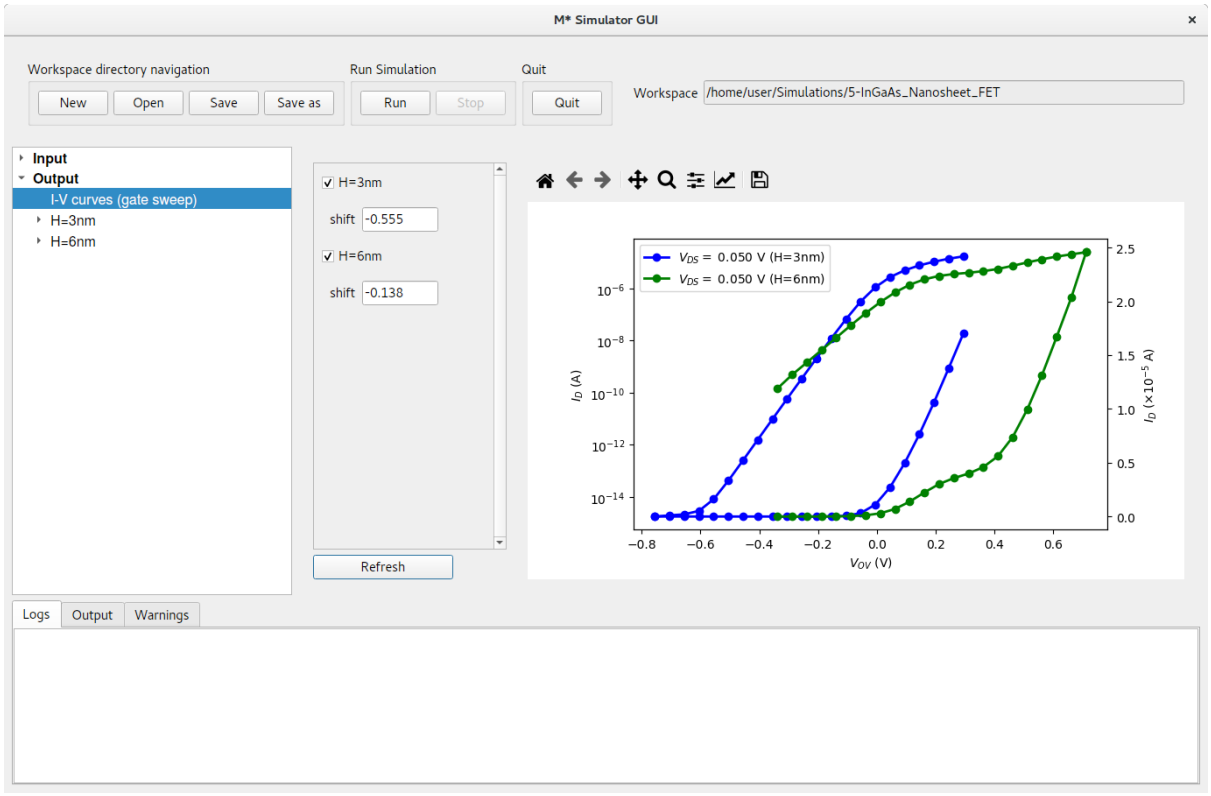


Figure 65: Comparison of both nanosheet device's transfer characteristics. Curves have been shifted such that their threshold voltage aligns with $V_G = 0$ V.

Figure 65 shows that the thicker device exhibits a larger subthreshold swing, and a lower ON current at the same *overdrive voltage* $V_{OV} = V_{GS} - V_{Th}$.[4] Comparing subthreshold swing values computed for both devices quantifies observed differences with the thicker device surpassing 100 mV/dec, while the thinner device exhibits values below 70 mV/dec. Inspecting 2D data for the thicker device's OFF states reveals the main reason behind this significantly different behaviour: OFF currents are dominated by source-to-drain current (e.g. fig. 66) whereas the thinner device's OFF currents are dominated by thermionic emission (e.g. fig. 58). This contrast is largely a consequence of the Γ valley's lower effective mass value along the transport direction.

[4]The horizontal axis' label has been manually set to $V_{OV}$ using the toolbar at the top of the plot.

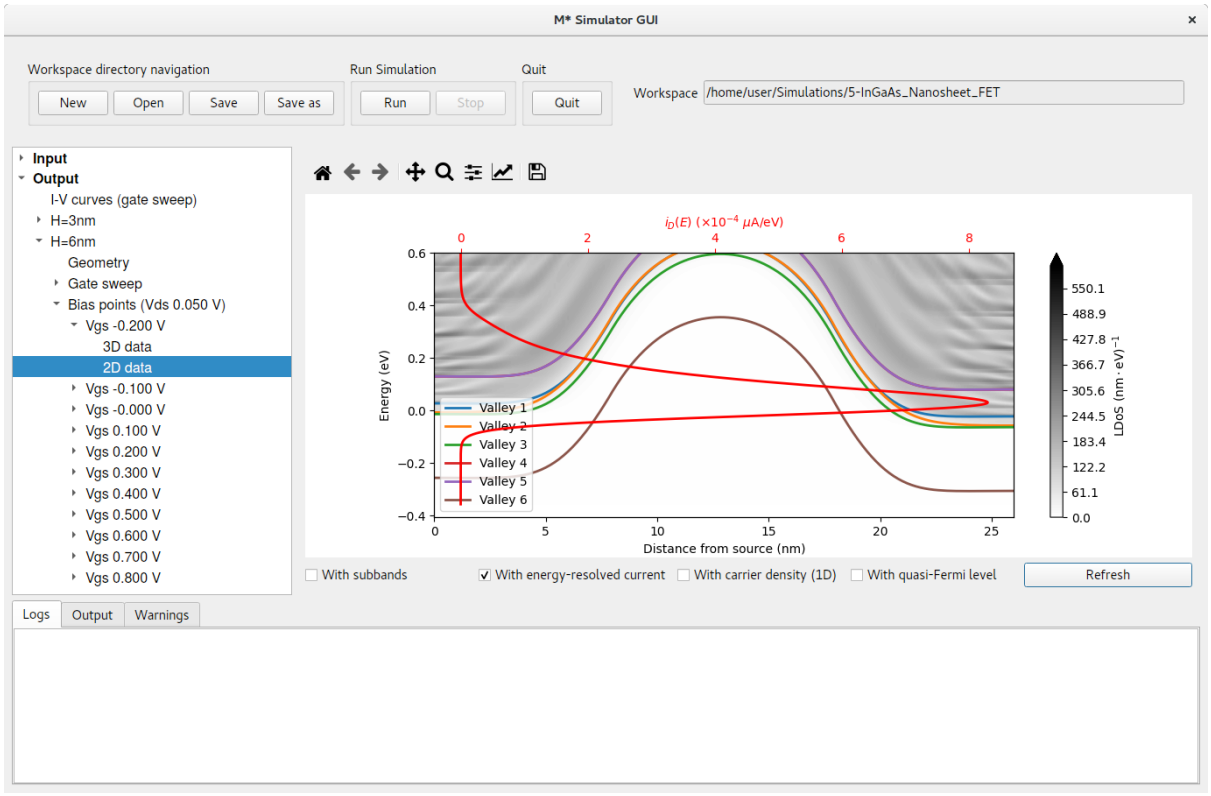


Figure 66: Local density of states, lowest subband for each valley, and energy-resolved current for the thicker device at $V_{GS} = -0.2$ V (OFF state).

# 6 Tutorial: Scattering in silicon nanowire FET

In this last test case we cover the inclusion of two types of scattering into $\mathcal{M}^*$ simulations: acoustic phonon scattering, and surface roughness scattering. We will employ the silicon nanowire FET structure simulated in section 1 with a channel length of 10 nm.

- If you have already followed the silicon nanowire FET tutorial, click `Open` in the $\mathcal{M}^*$ GUI's top pane and select the corresponding workspace's top folder to load all associated data and append the results from this tutorial into it
- If you have not yet followed the silicon nanowire FET tutorial, click `Open` in the $\mathcal{M}^*$ GUI's top pane and select an empty folder. See section 1 for instructions on how to set up the input parameters for a ballistic simulation

## 6.1 Acoustic phonon scattering

Using input parameters employed for the first simulation described in section 1 as a starting point, click on `Input->Control` and set `Scattering: Acoustic`, as shown below. Click `Run` to begin the simulation.

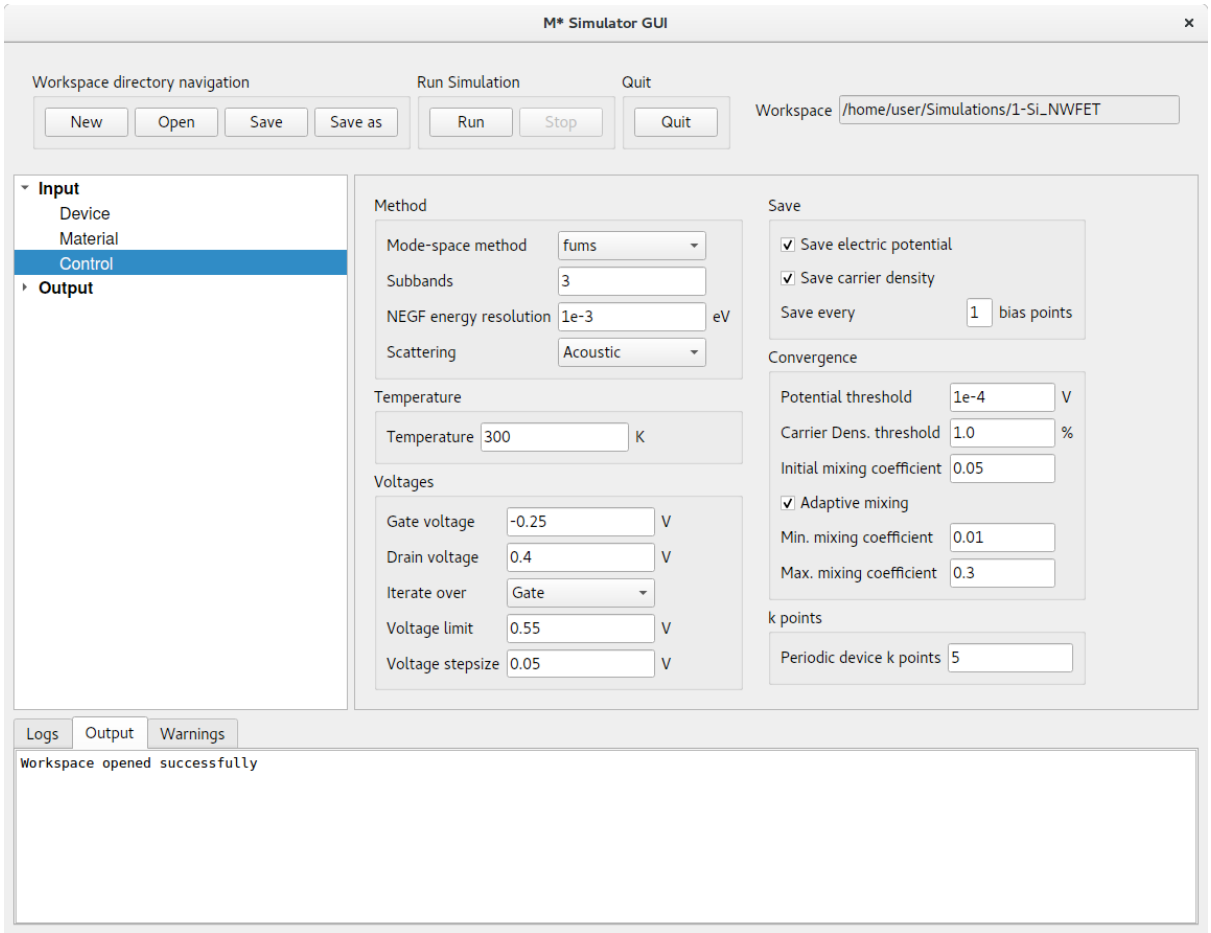


Figure 67: In the `Control` panel, select `Acoustic` from the `Scattering` dropdown menu.

Once finished, you can compare the effects of including acoustic phonon scattering in your simulation. In `Output->I-V curves (gate sweep)`, compare transfer characteristics by selecting only this most recent simulation and its corresponding ballistic equivalent from the list on the left. Figure 68 shows the resulting plot; although both curves exhibit the same general characteristics and subthreshold slope, the simulation including scattering from acoustic phonons shows lower current. Inspection of the data shows scattering lowers the drain current, with larger drops observed for ON states.

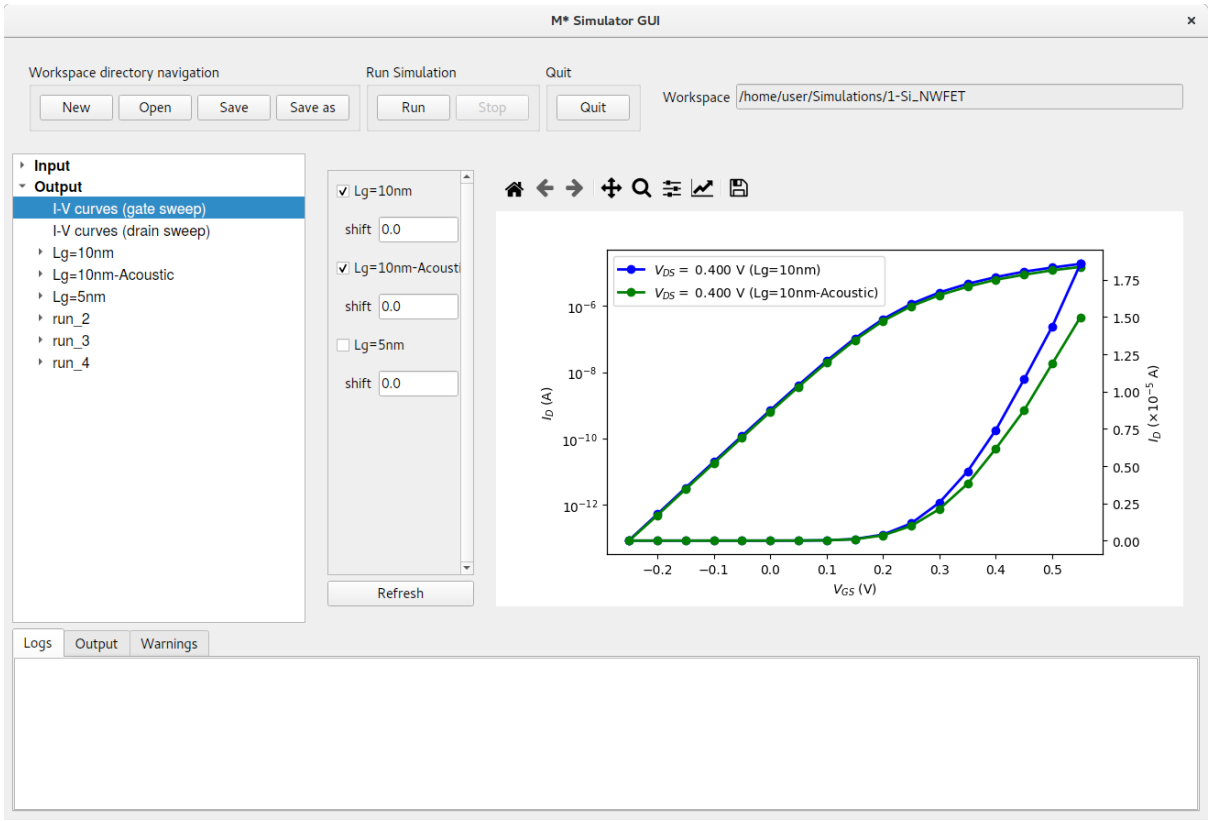


Figure 68: Transfer characteristics of silicon nanowire FET with acoustic phonon scattering, and in the ballistic approximation.

## 6.2 Surface roughness scattering

To include the scattering induced by surface roughness in your simulation, $\mathcal{M}^*$ explicitly generates a surface roughness profile along your device. This approach is preferred to employing ensemble averages for short-channel devices where lengths may not allow for statistical averages to hold; furthermore, this methodology allows studying variations between different individual devices in more detail.

To enable roughness in your device geometry, click on `Input->Device` and find the `Surface roughness` variables at the top right. As shown in fig. 69, we shall input an RMS amplitude of 0.2 nm, a correlation length of 1.0 nm and choose an exponential autocorrelation function for the generation of the profile. The `Manual seed` field allows some control over the random number generator employed when generating the profile; input a value of 10 to obtain the same profile studied in this tutorial or leave blank to

use a seed based on your system's clock.[5]

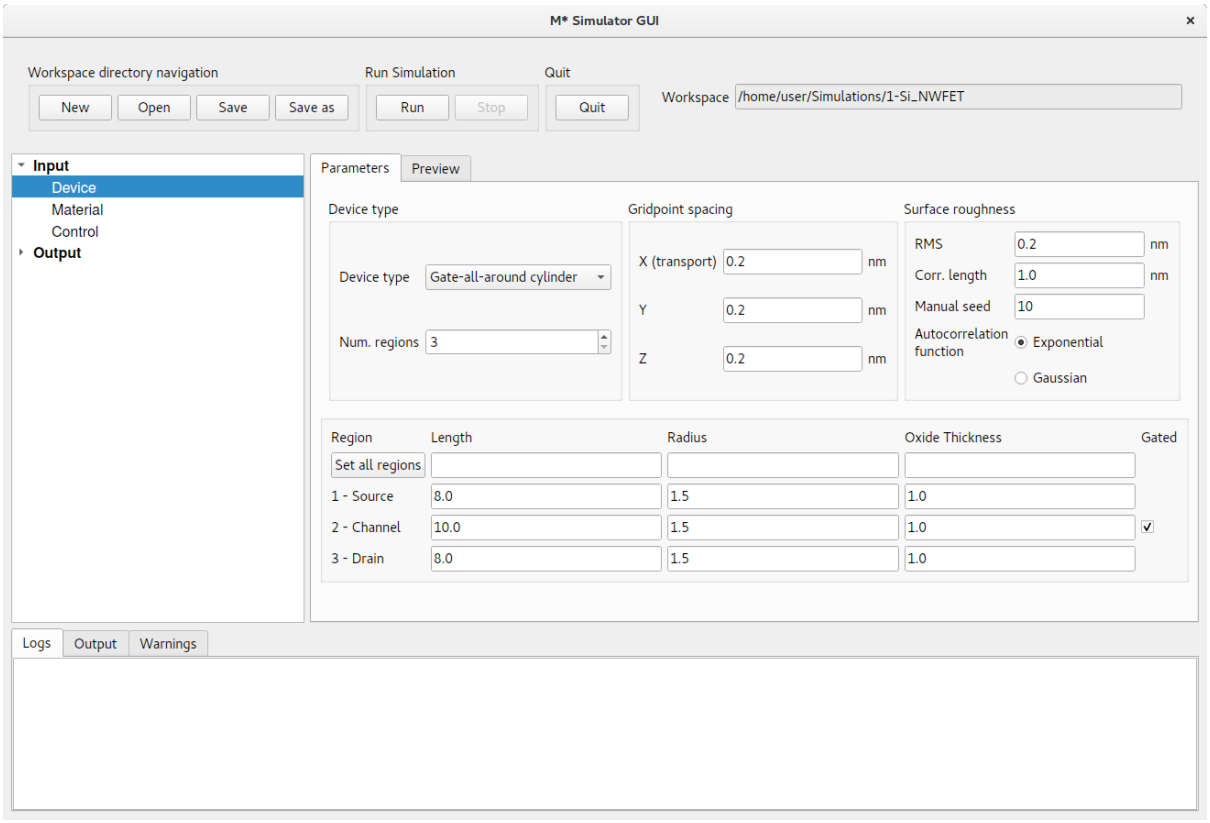


Figure 69: In the `Device` panel, input variables shown above in the `Surface roughness` section at the top right.

Finally, click on `Input->Control` and select CMS as mode-space method; cross-sectional inhomogeneities produced by the roughness profile require coupling between modes in adjacent slices to be explicitly computed. Ensure `Scattering` is set to ballistic in order to be able study the effects of surface roughness and acoustic scattering separately later on. Click `Run` when you are ready to begin the simulation.

[5]Note: the geometry preview tab does not show surface roughness profiles; you may only visualise the structure including surface roughness in the `Output` section.

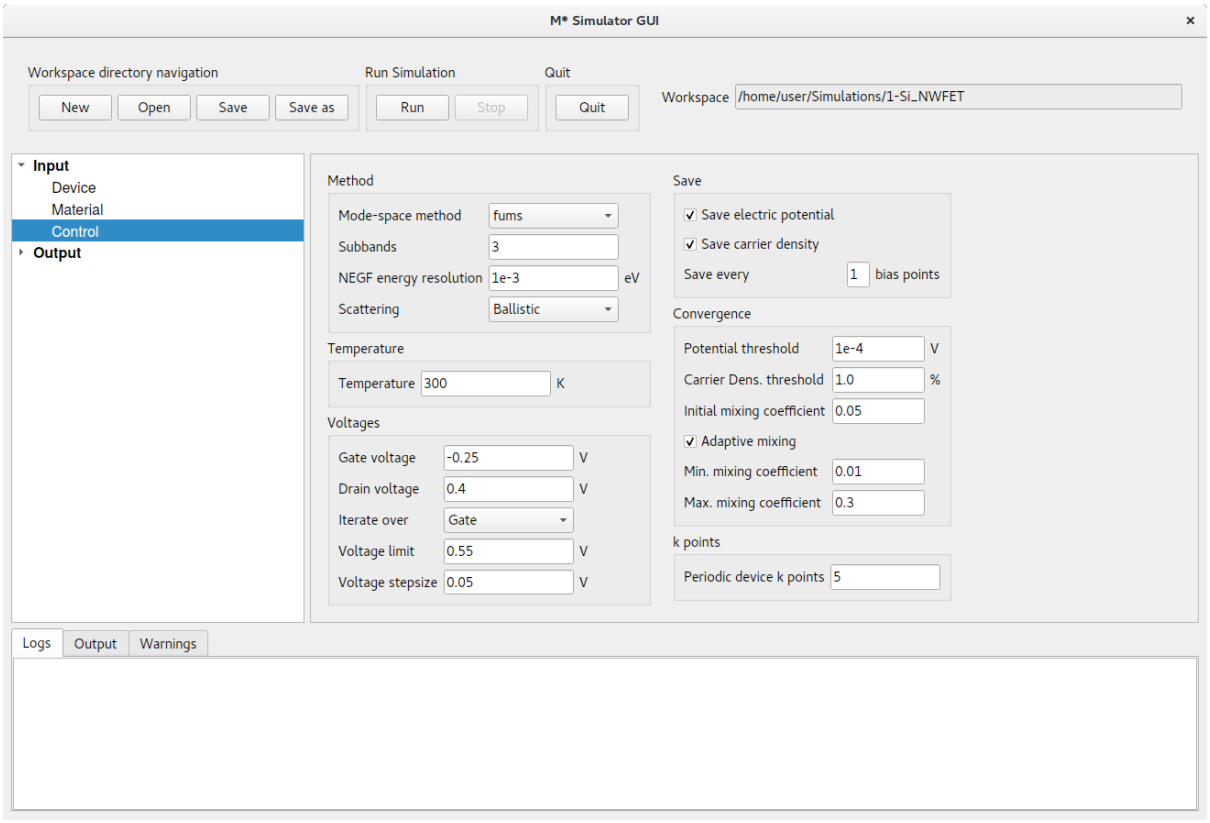


Figure 70: In the `Control` panel, select the CMS mode-space method and ballistic scattering.

You may visualise the geometry output once a first bias point has converged (Figure 71). Note only the device channel exhibits a roughness profile. In general, surface roughness profiles are generated for all device regions except source and drain extensions (i.e. first and last geometry regions).

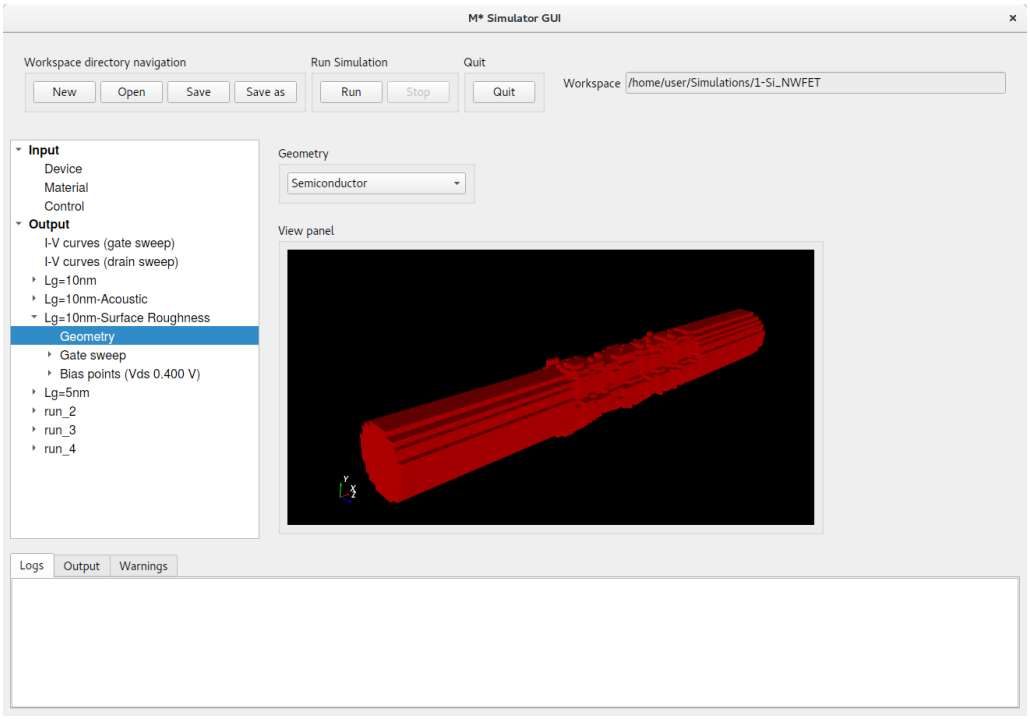


Figure 71: Geometry (semiconductor only) of simulated device including surface roughness profile in the channel.

Once your simulation has completed, you may include $I_D - V_{GS}$ characteristics in the comparison performed in the previous section. Compare transfer characteristics using `Output->I-V curves (gate sweep)` by selecting both curves plotted in fig. 68 and the surface roughness curve. Figure 72 shows a comparison between the three cases: ballistic, acoustic phonon scattering, and surface roughness scattering; it is clear that scattering induced by the surface roughness profile is larger than that induced by acoustic phonon modes. Note that curves have been shifted by their threshold voltage in order to compare them in a meaningful way, as illustrated in the previous tutorial.

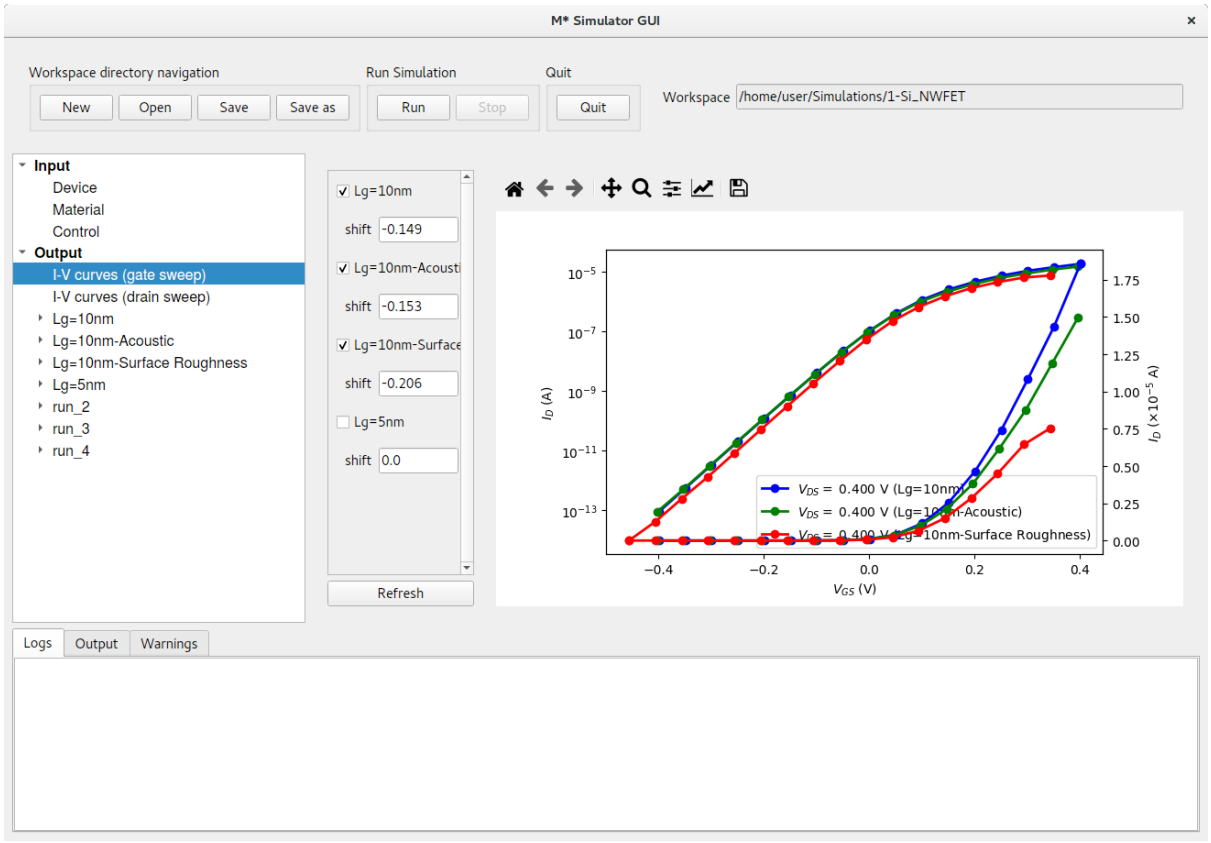


Figure 72: Shifting curves to make threshold voltages coincide allows meaningful comparisons. The simulated surface roughness profile degrades current more than acoustic phonon scattering in the smooth device.

To finalise this tutorial, let us investigate the effects of both types of scattering on carrier density throughout the device, energy-resolved current, and local density of states. Figures 73 to 75 show the corresponding 2D data plots near their threshold voltages. Note limits on energy-resolved horizontal axes have been edited using each plot's toolbar in order to facilitate comparisons.

- **Acoustic phonon scattering** reduces oscillations and resonances in the LDoS, resulting in a smoothed contour plot when compared to the ballistic case. Back scattering of carriers by phonon modes results in a reduction of carrier density in the channel, as well as a reduced energy-resolved current
- **Surface roughness scattering** reduces oscillations and resonances in the LDoS, similar to the acoustic phonon scattering case. Variations in subband energies across different slices result in channel regions with localised states, shown as darker regions in the LDoS plot; their impact can also be observed as fluctuations in the carrier density along the channel not present in the smooth device. Local barriers induced by subband energy variations impose tunnelling barriers on carriers travelling through certain regions of the channel and reduce the magnitude of the energy-resolved current.

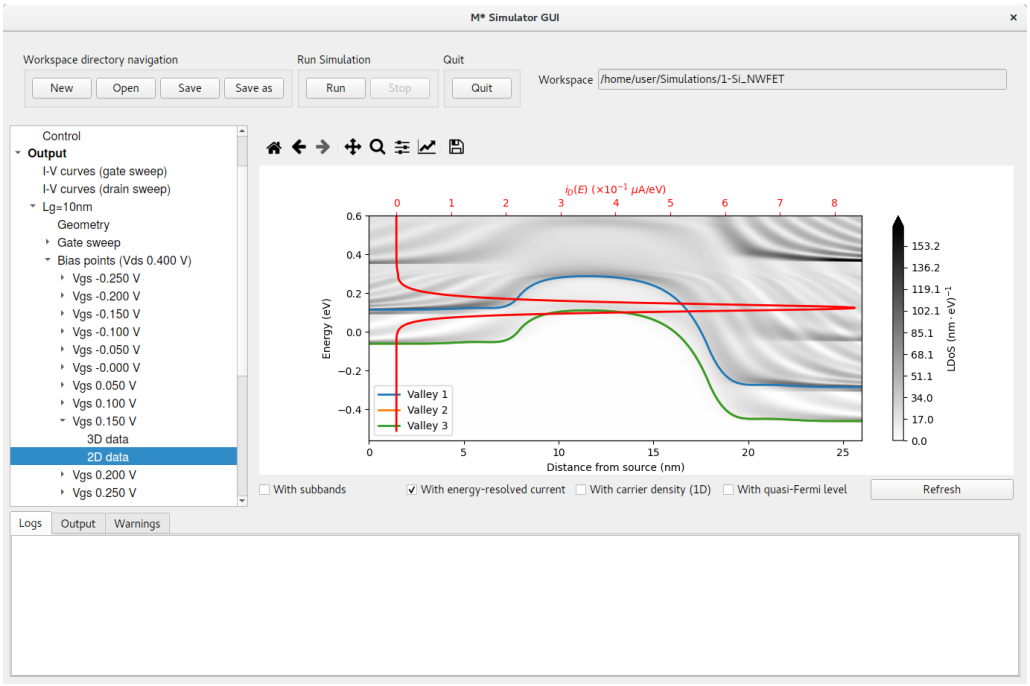


Figure 73: Local density of states and energy-resolved current for the ballistic simulation near its threshold voltage.

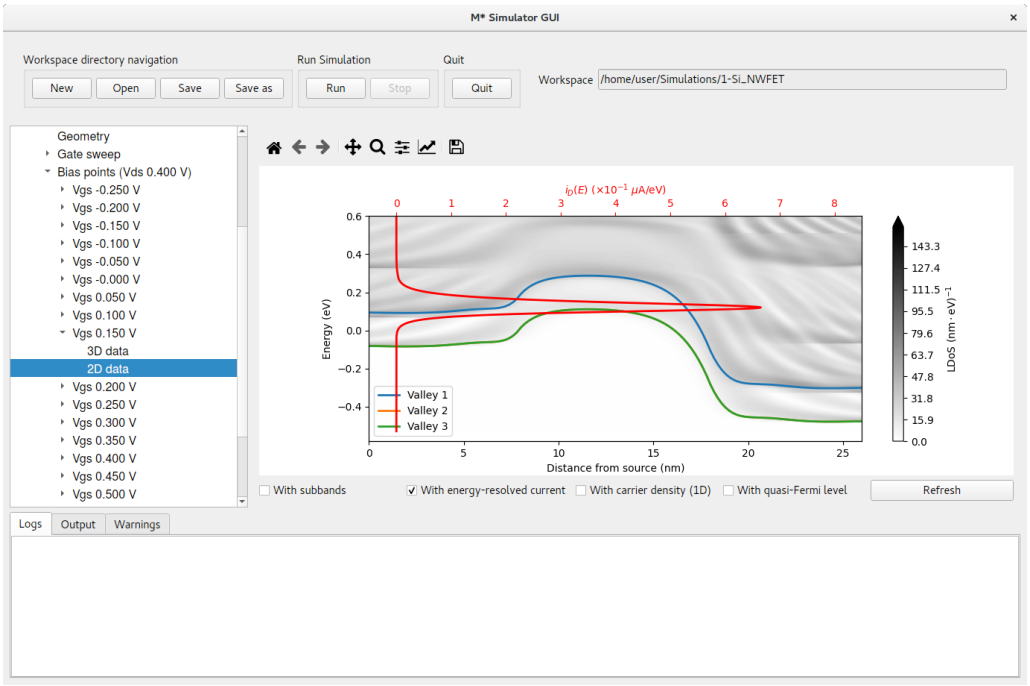


Figure 74: Local density of states and energy-resolved current for the simulation with acoustic phonon scattering near its threshold voltage.

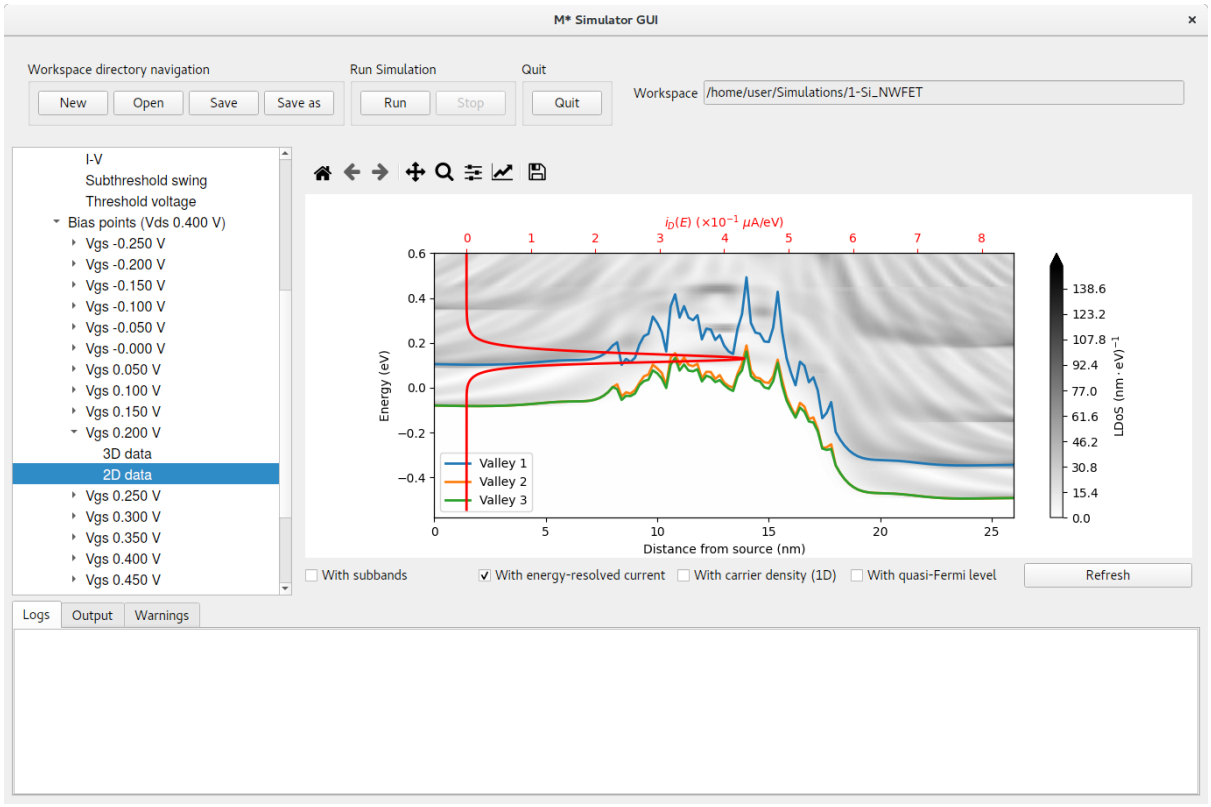


Figure 75: Local density of states and energy-resolved current for the simulation including surface roughness near its threshold voltage.

# References


[1] D. K. Schroder, *Semiconductor Material and Device Characterization*. John Wiley & Sons, Inc., apr 2005.

[2] U. Ayachit, *The ParaView Guide: A Parallel Visualization Application*. Kitware, Incorporated, 2015.

[3] "https://www.paraview.org/."

[4] J.-S. Park, J. Bai, M. Curtin, B. Adekore, M. Carroll, and A. Lochtefeld, "Defect reduction of selective ge epitaxy in trenches on si(001) substrates using aspect ratio trapping," *Applied Physics Letters*, vol. 90, p. 052113, jan 2007.

[5] N. D. Akhavan, A. Afzalian, C.-W. Lee, R. Yan, I. Ferain, P. Razavi, R. Yu, G. Fagas, and J.-P. Colinge, "Nanowire to single-electron transistor transition in trigate SOI MOSFETs," *IEEE Transactions on Electron Devices*, vol. 58, pp. 26–32, jan 2011.